

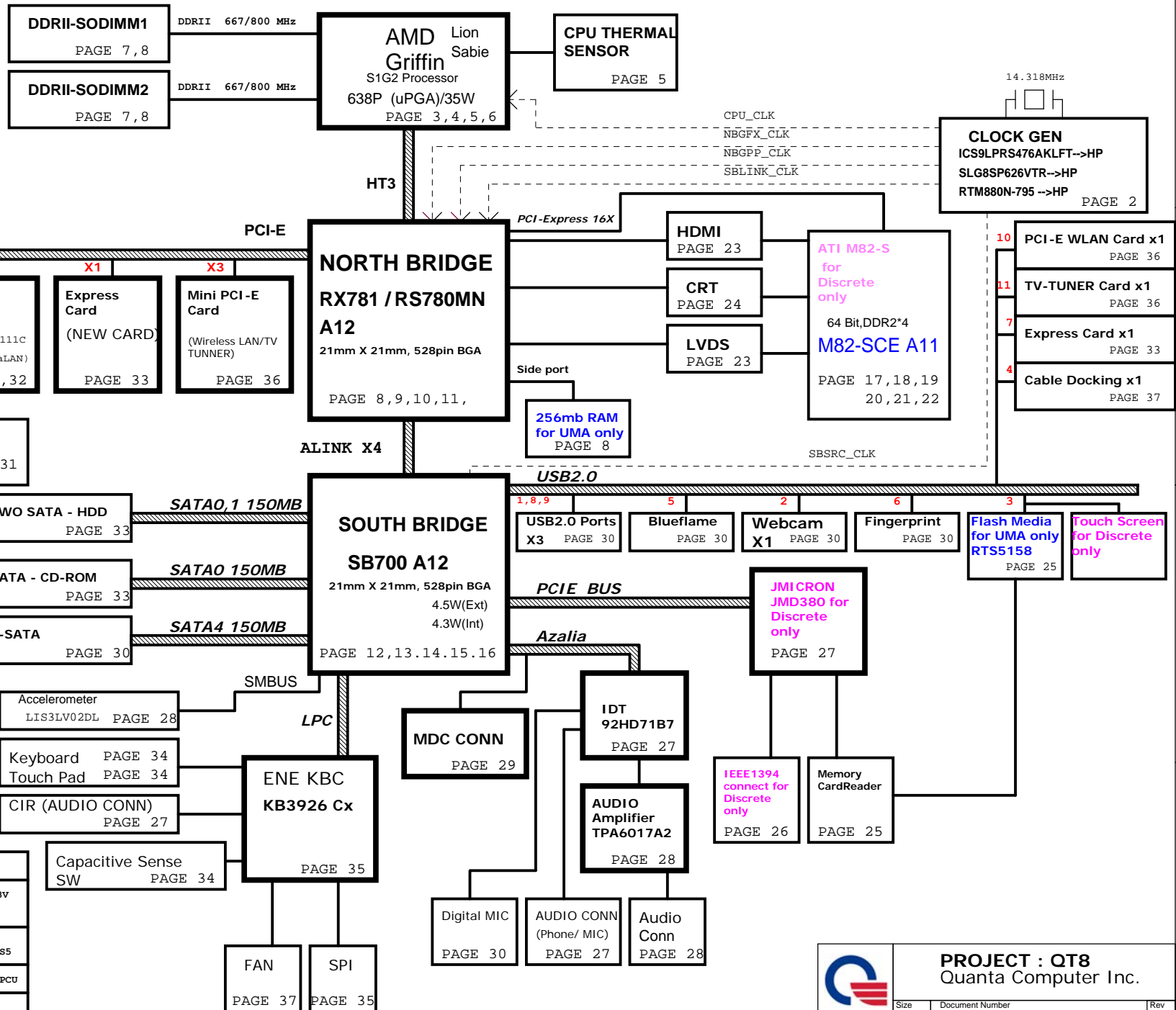
# QT8 SYSTEM DIAGRAM

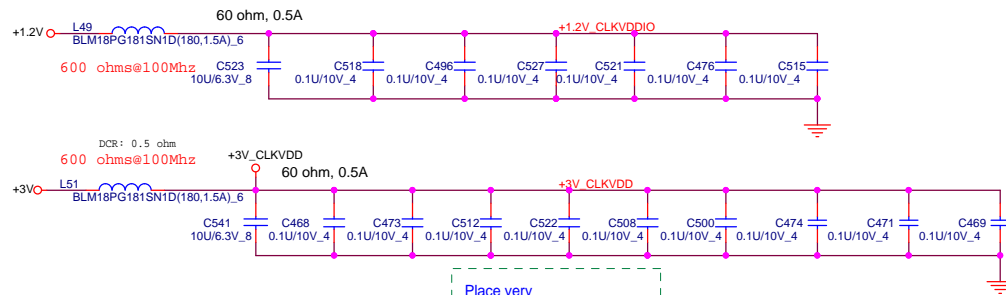


01

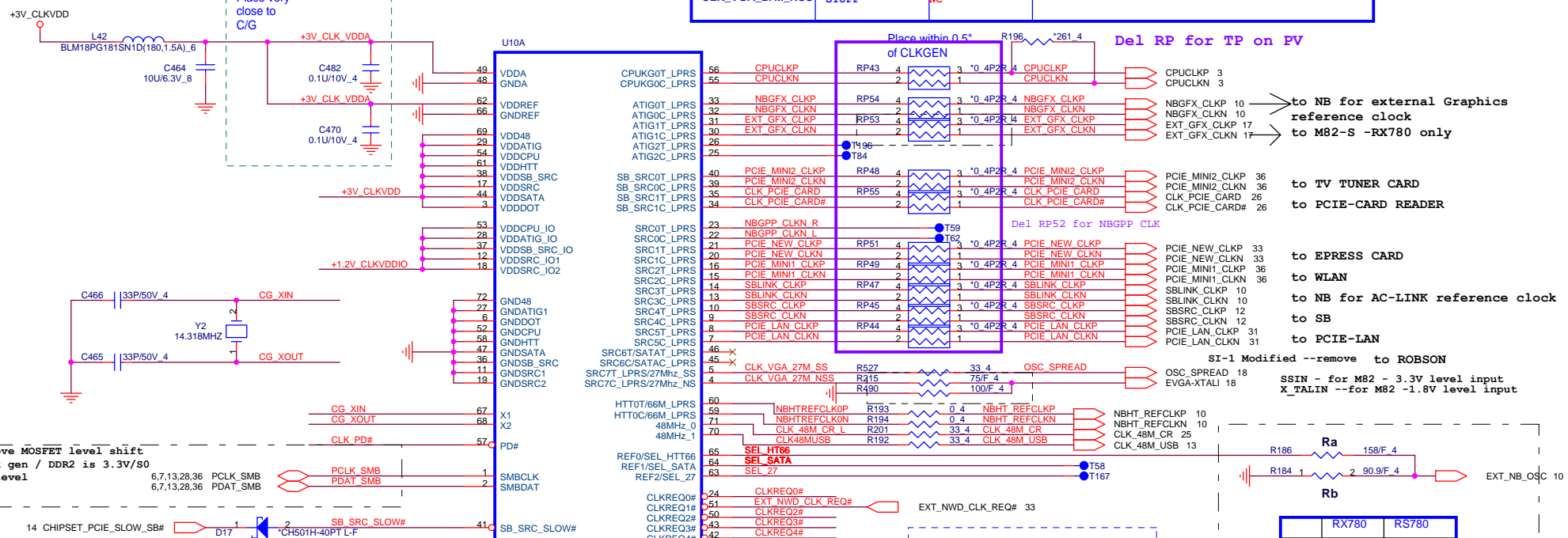
## PCB STACK UP

LAYER 1 : TOP  
LAYER 2 : IN1  
LAYER 3 : IN2  
LAYER 4 : VCC  
LAYER 5 : IN3  
LAYER 6 : BOT

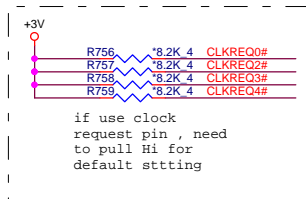
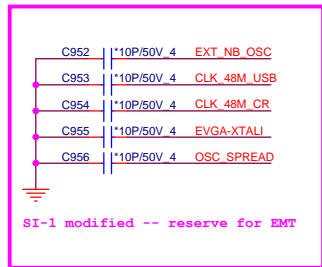




CLOCKS name	RX780	RS780	Clock pin function
NBGF_X_CLKP NBGF_X_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP66 STUFF	RP66 NC	to M82-S external reference clock -RX780 only
NBGP_P_CLKP NBGP_P_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock, RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock
CLK_VGA_27M_SS CLK_VGA_27M_NSS	R653, R656, R612 STUFF	R653, R656, R612 NC	To M82-S 27Mhz - RX780 only

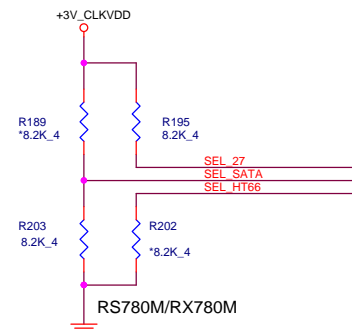


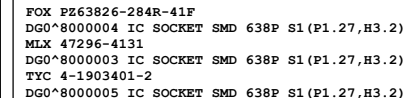
when driven lowSB\_SRC clocks slow only supported with  
to reduced setpoint custom CG IC



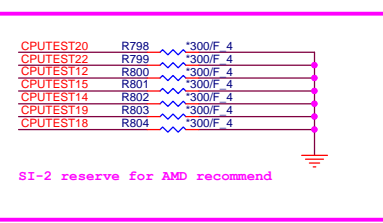
ICS ICS9LPR476BKLFT--AJRS4760000  
SLG SLG8SP626VTR--AJ006260000  
RTL RTL880N-795-- AJ008800000

* default		
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock



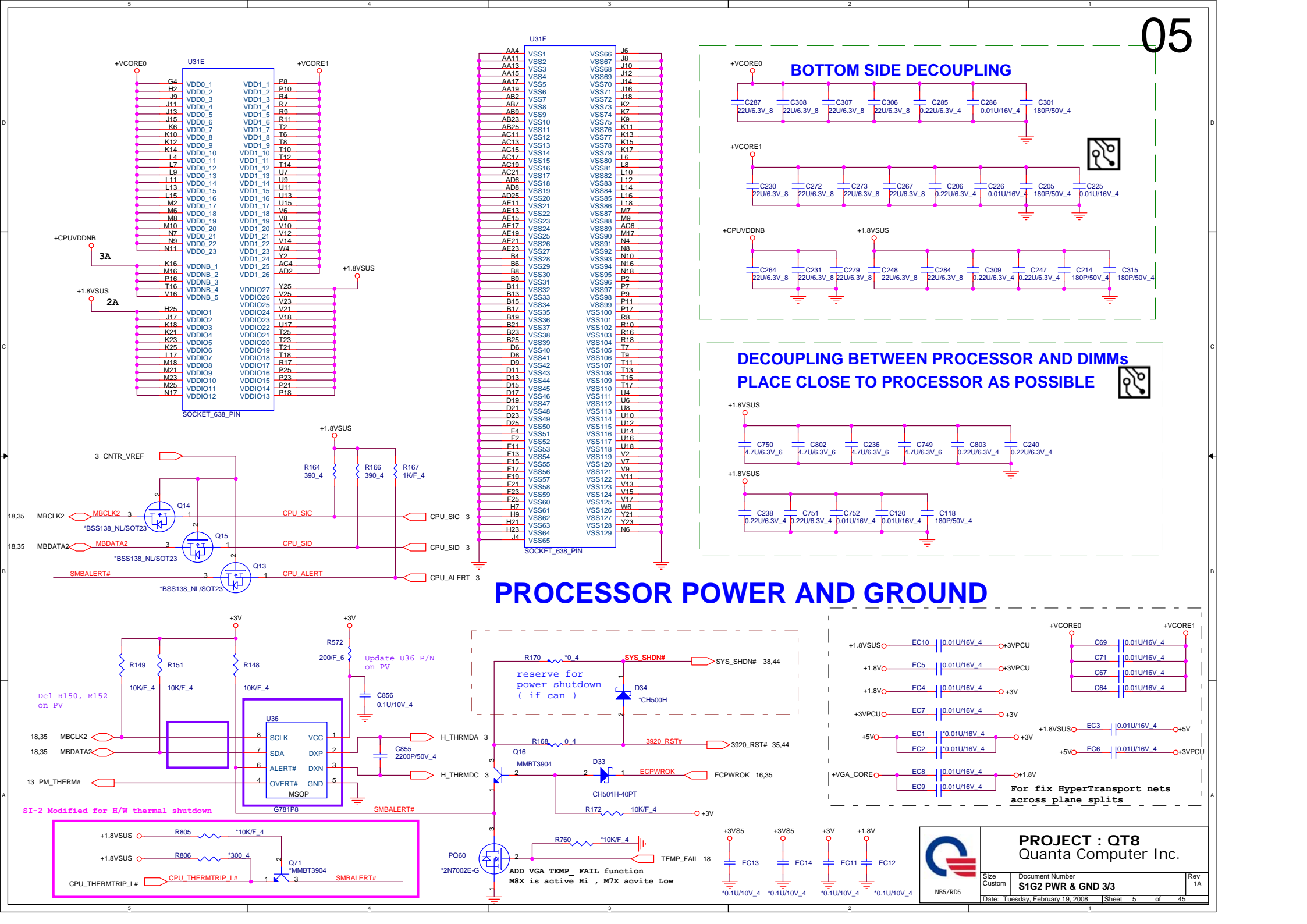


## HDT Connector

VFIX MODE VID Override Circuit



Size Custom	Document Number <b>S1G2 DDRII MEMORY I/F 2/3</b>	R
Date: Tuesday, February 19, 2008	Sheet 4 of 45	



05

**PROCESSOR POWER AND GROUND**

**TOP SIDE DECOUPLING**

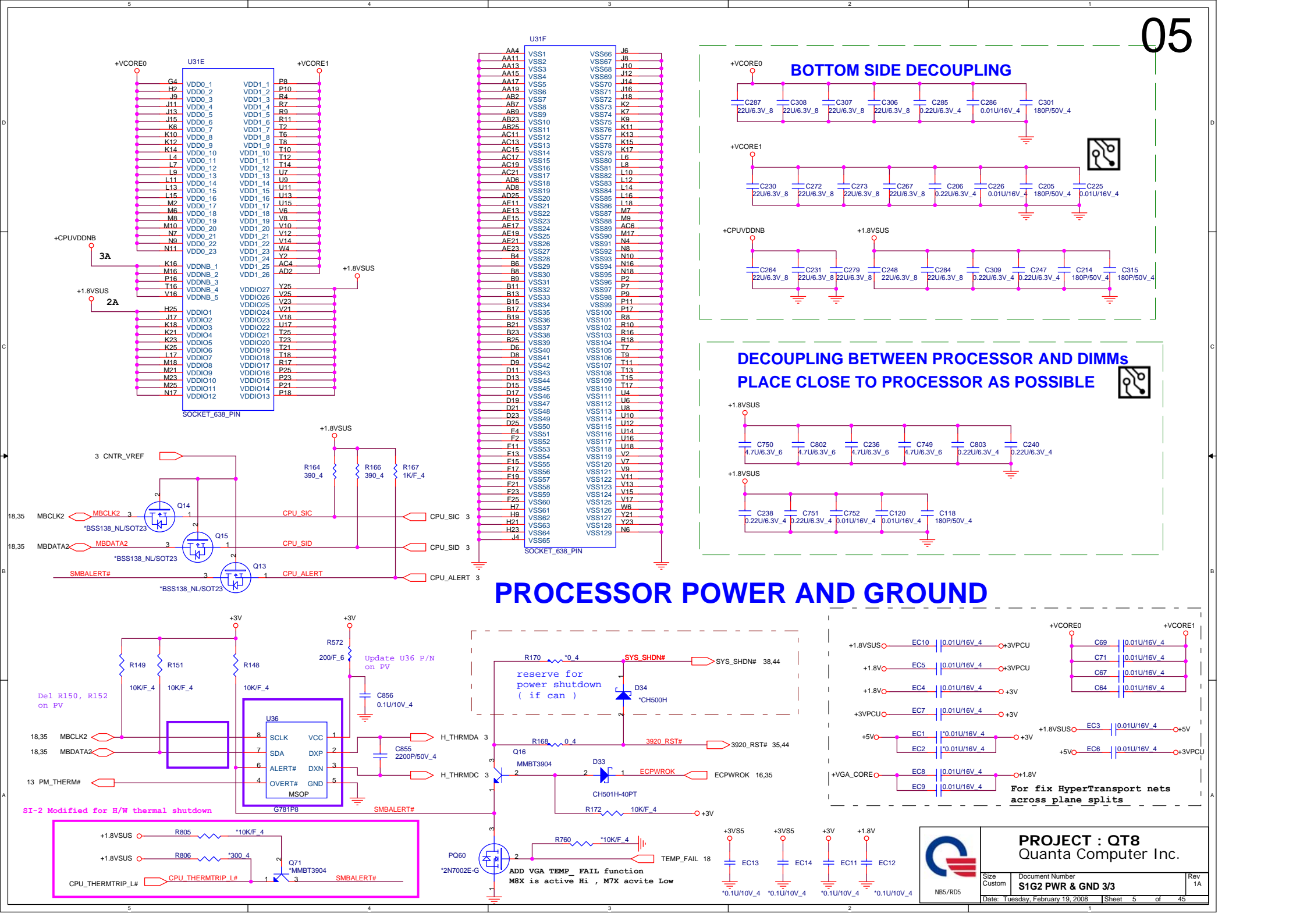
**BOTTOM SIDE DECOUPLING**

**DECOUPLING BETWEEN PROCESSOR AND DIMMs**  
PLACE CLOSE TO PROCESSOR AS POSSIBLE

**PROCESSOR POWER AND GROUND**

**PROJECT : QT8**  
Quanta Computer Inc.

Size Custom Document Number S1G2 PWR & GND 3/3 Rev 1A  
Date: Tuesday, February 19, 2008 Sheet 5 of 45



05

**PROCESSOR POWER AND GROUND**

**TOP SIDE DECOUPLING**

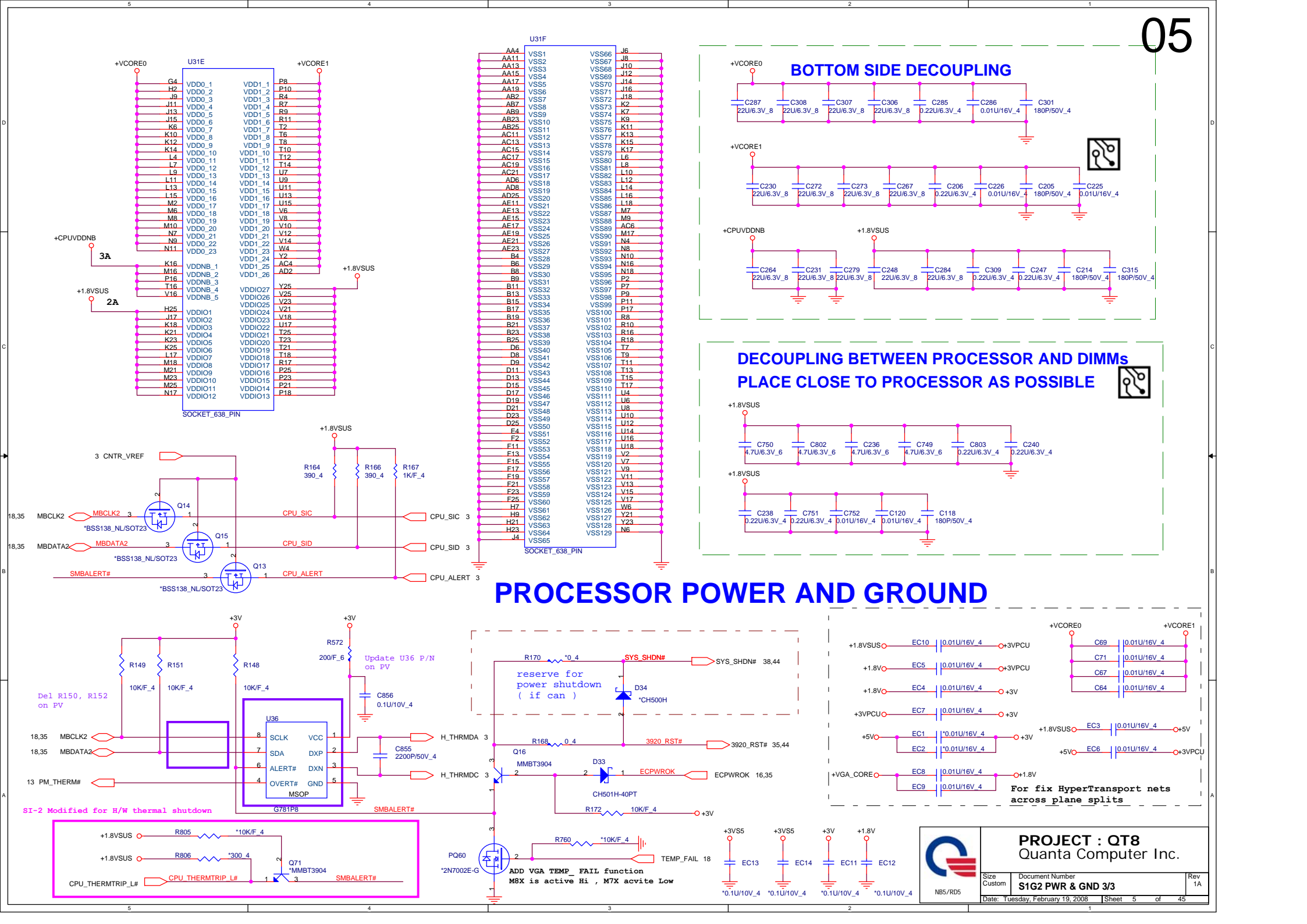
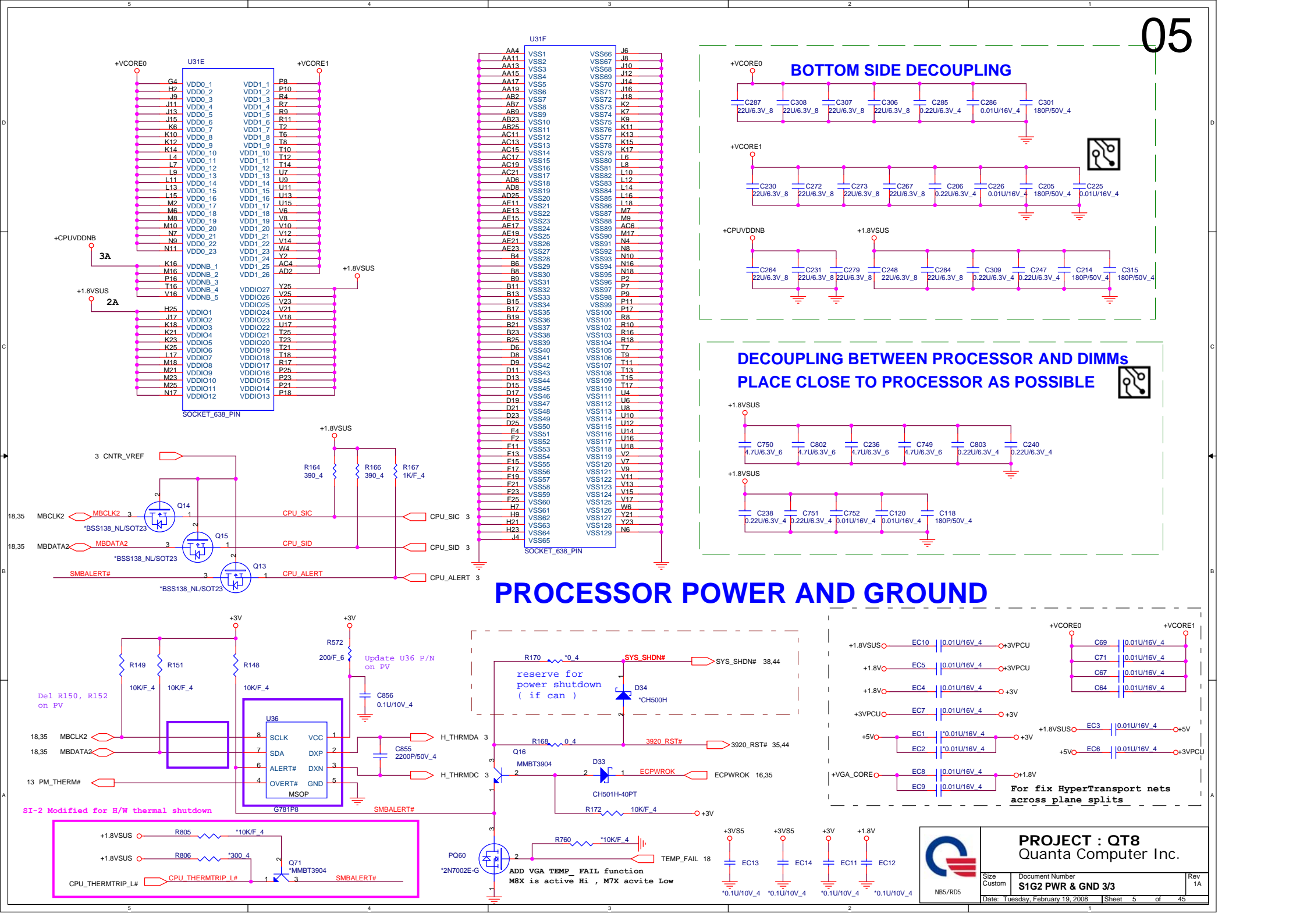
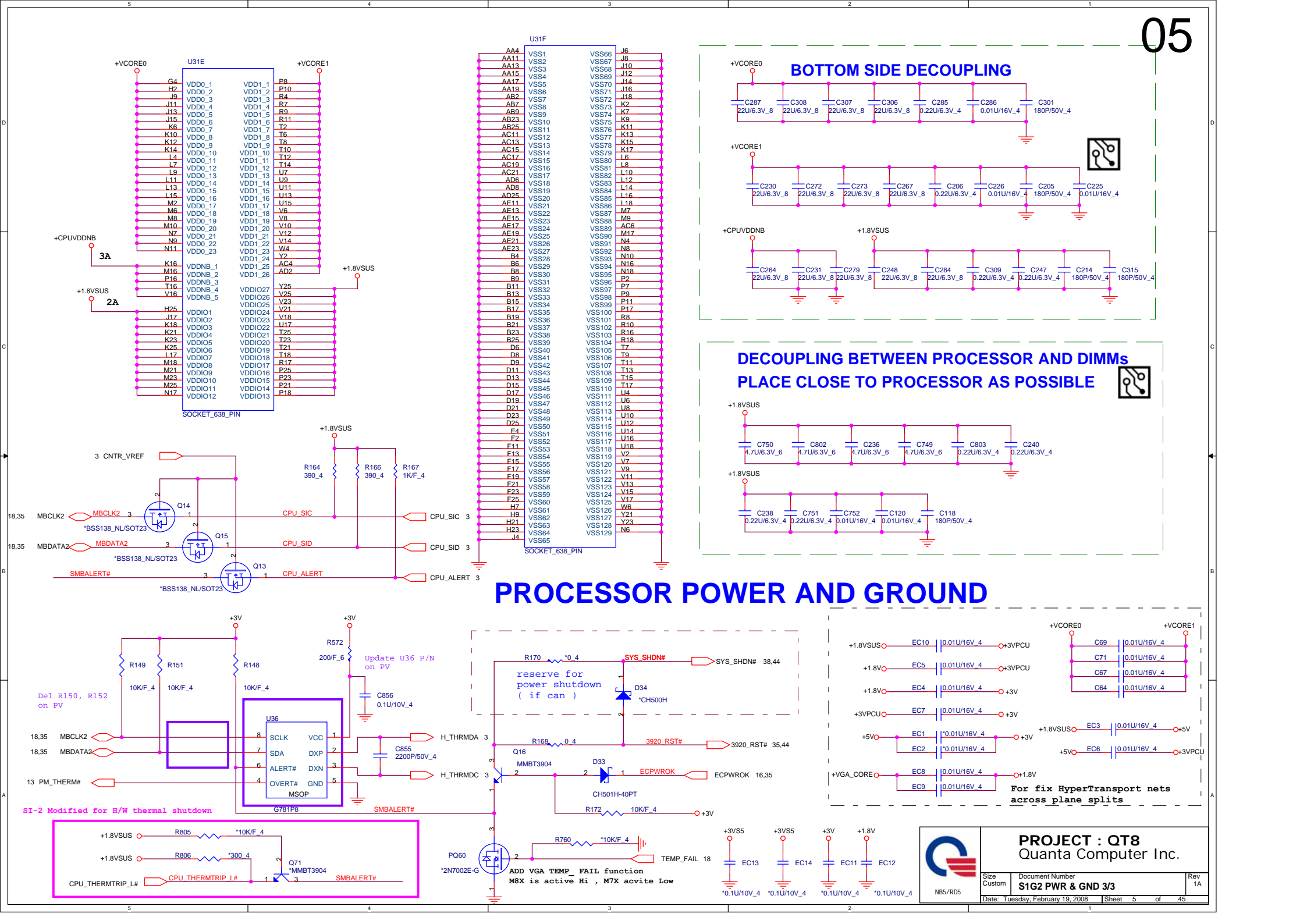
**BOTTOM SIDE DECOUPLING**

**DECOUPLING BETWEEN PROCESSOR AND DIMMs**  
PLACE CLOSE TO PROCESSOR AS POSSIBLE

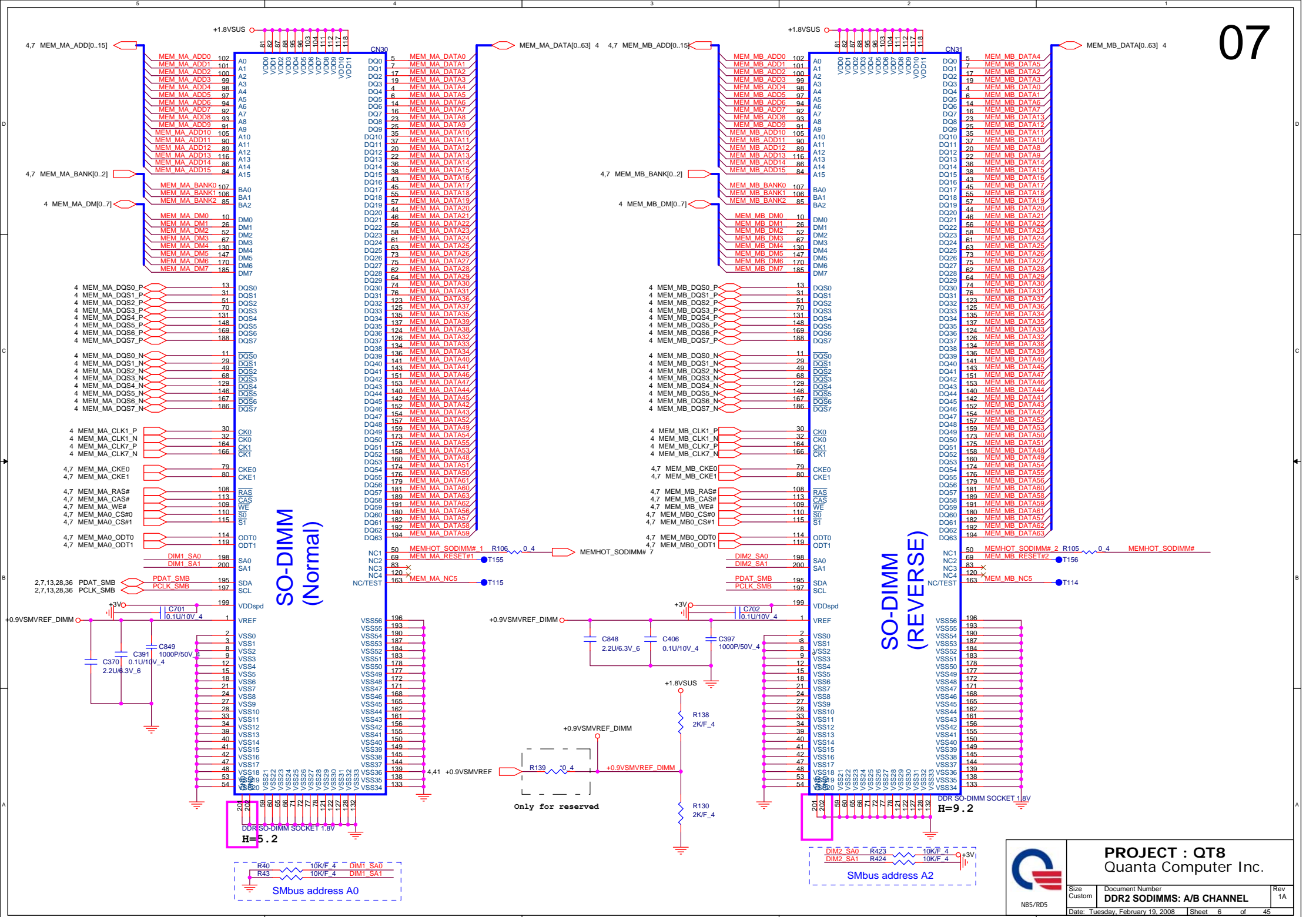
**PROCESSOR POWER AND GROUND**

**PROJECT : QT8**  
Quanta Computer Inc.

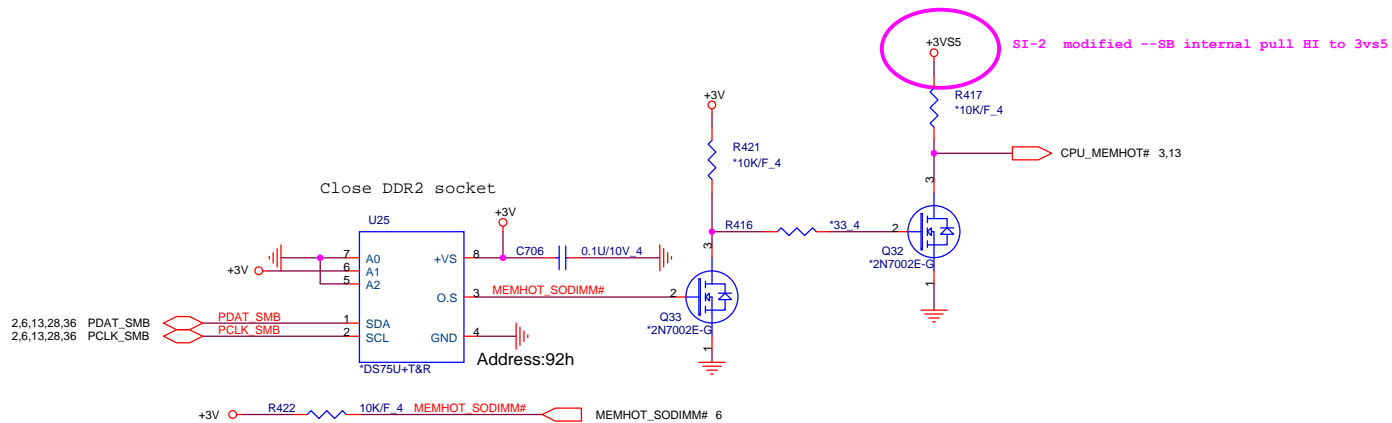
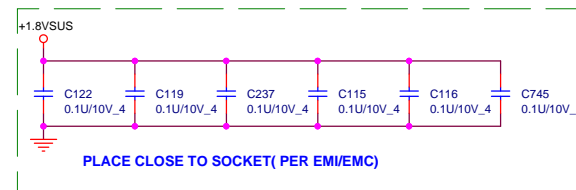
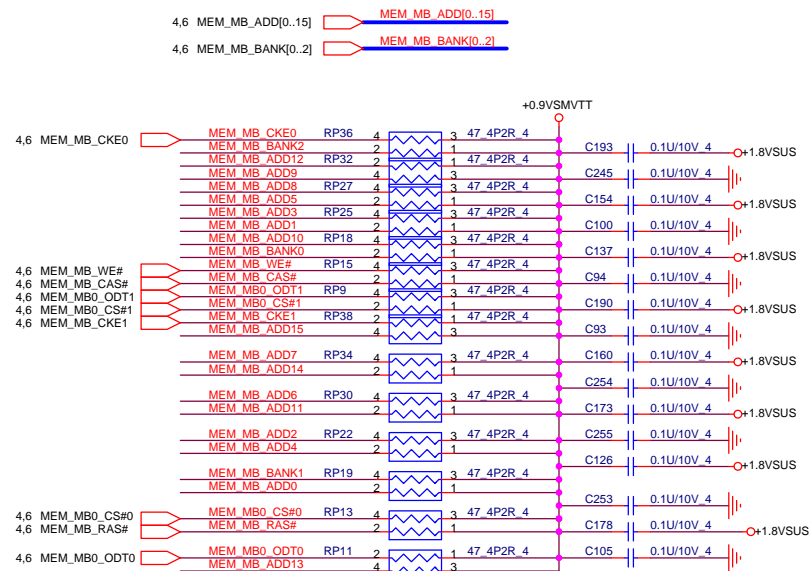
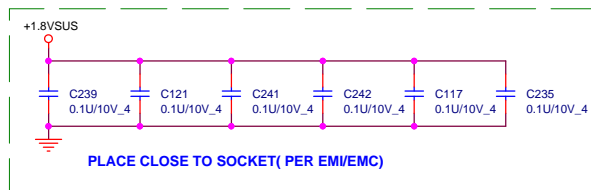
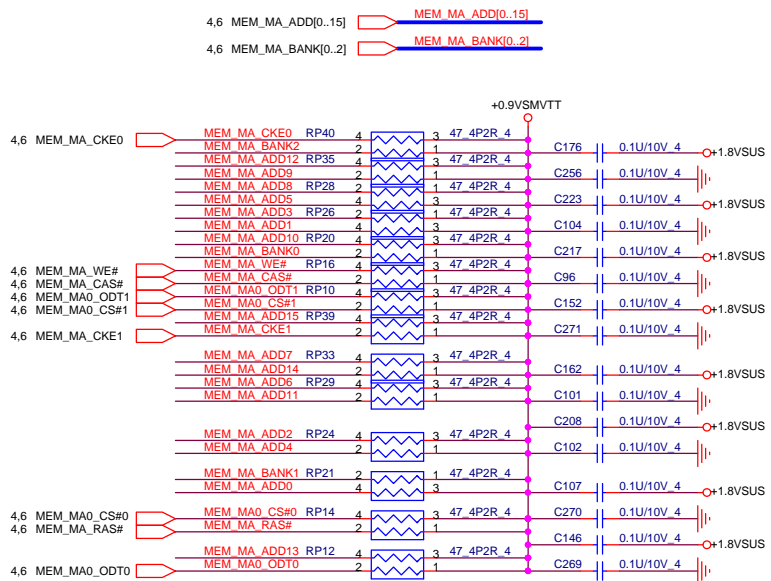
Size Custom Document Number S1G2 PWR & GND 3/3 Rev 1A  
Date: Tuesday, February 19, 2008 Sheet 5 of 45

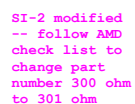






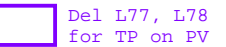
PROJECT : QT8  
Quanta Computer Inc.



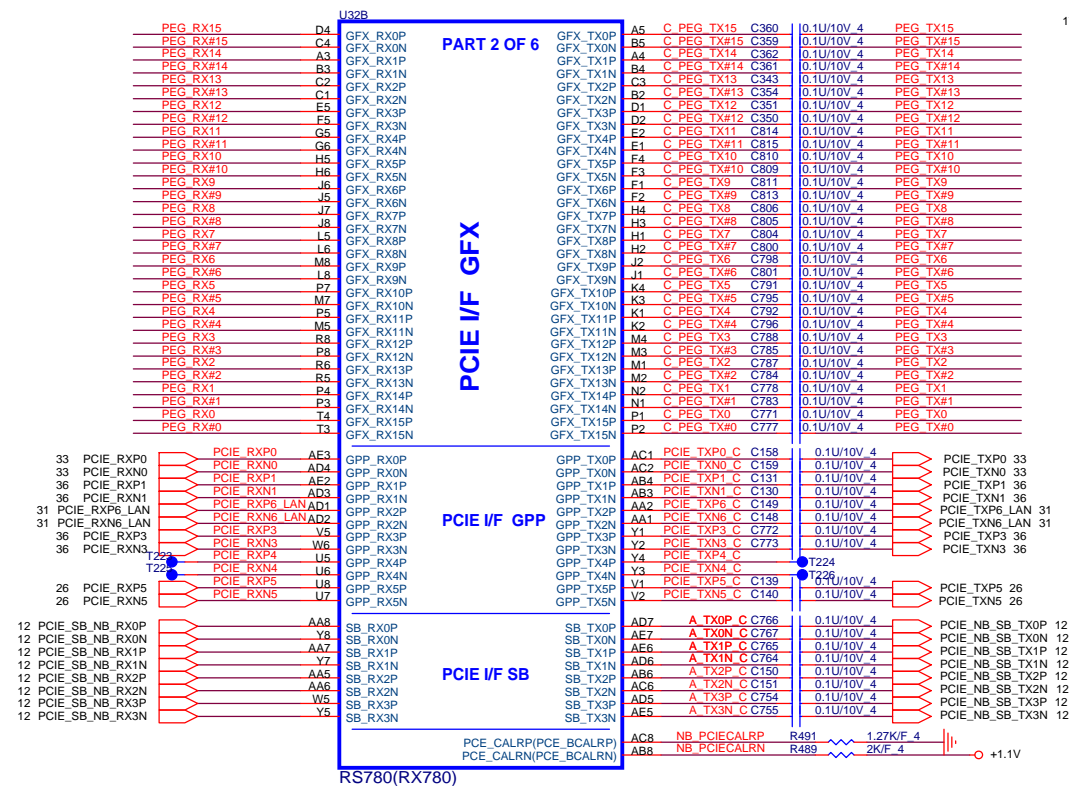


RES CHIP 1.21K 1/16W +-1% (0402)  
P/N : CS21212FB18

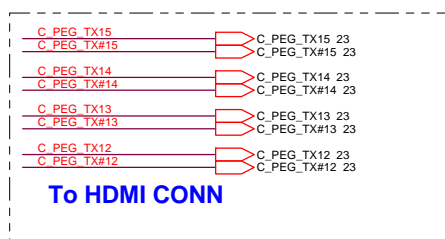
RES CHIP 301 1/16W +-1% (0402)  
P/N : CS13012FB14







Close to North Bridge



TO EXPRESS CARD

TO WLAN

TO PCIE-LAN

TO TV TUNNER

TO PCIE CARD READER

RX780/RS740/RS780 difference table (PCIE LINK)

	RS740	RX780/RS780
NB_PCIECALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

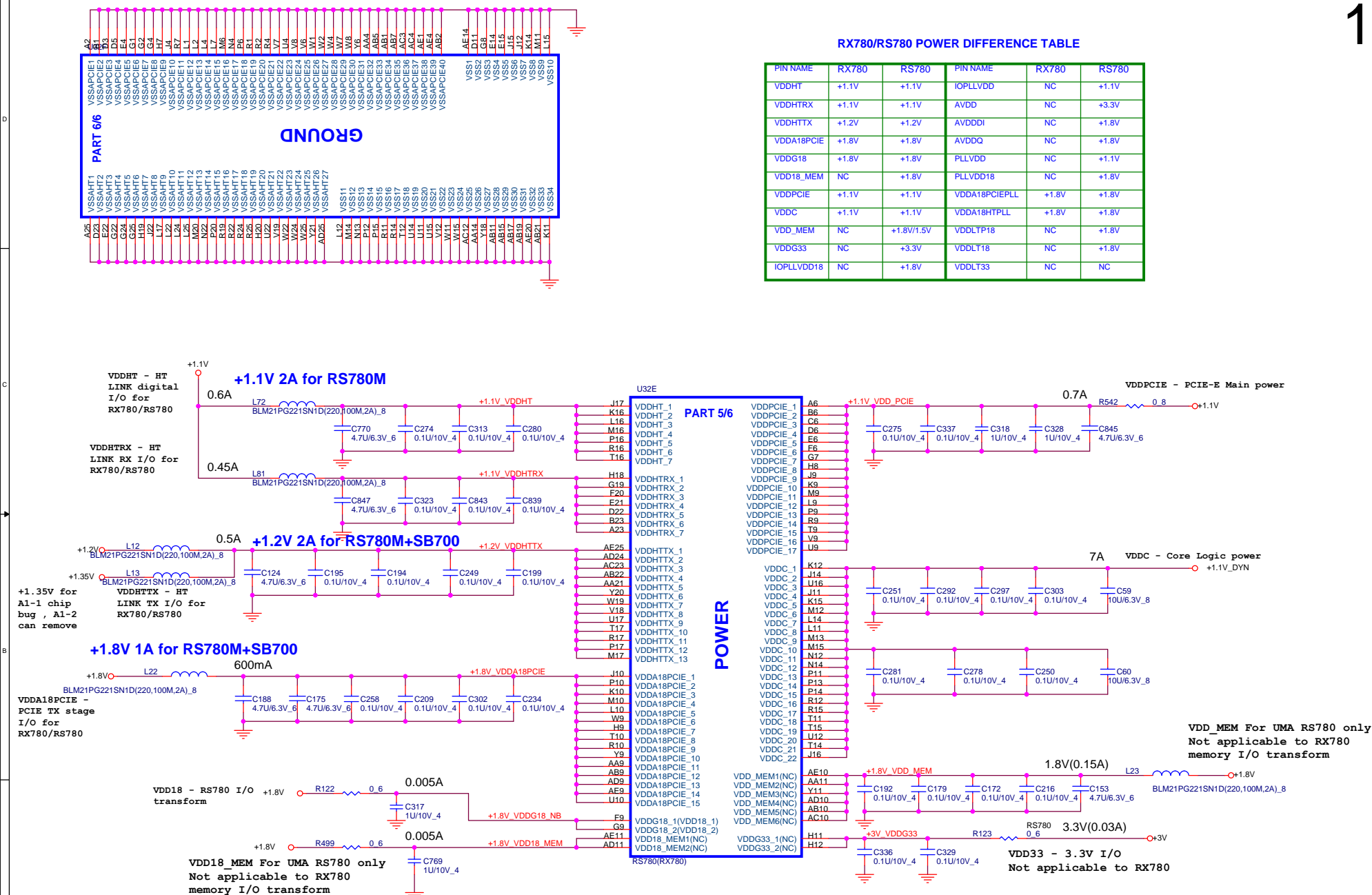


**PROJECT : QT8**  
Quanta Computer Inc.



### RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVD0	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD0	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD018	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVD018	NC	+1.8V	VDDL133	NC	NC

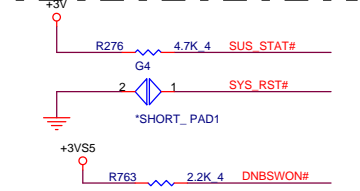
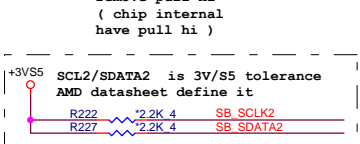
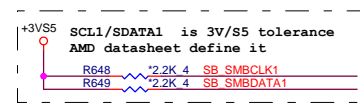
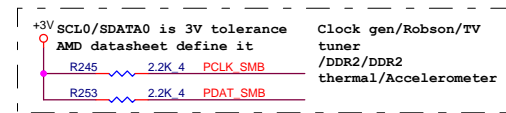
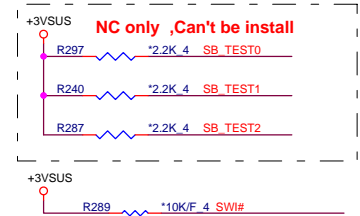


**PROJECT : QT8**  
Quanta Computer Inc.

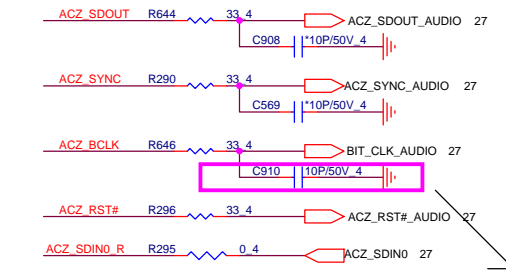
Size Custom	Document Number <b>RS740/RS780-POWER5/5</b>
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Rev  
14

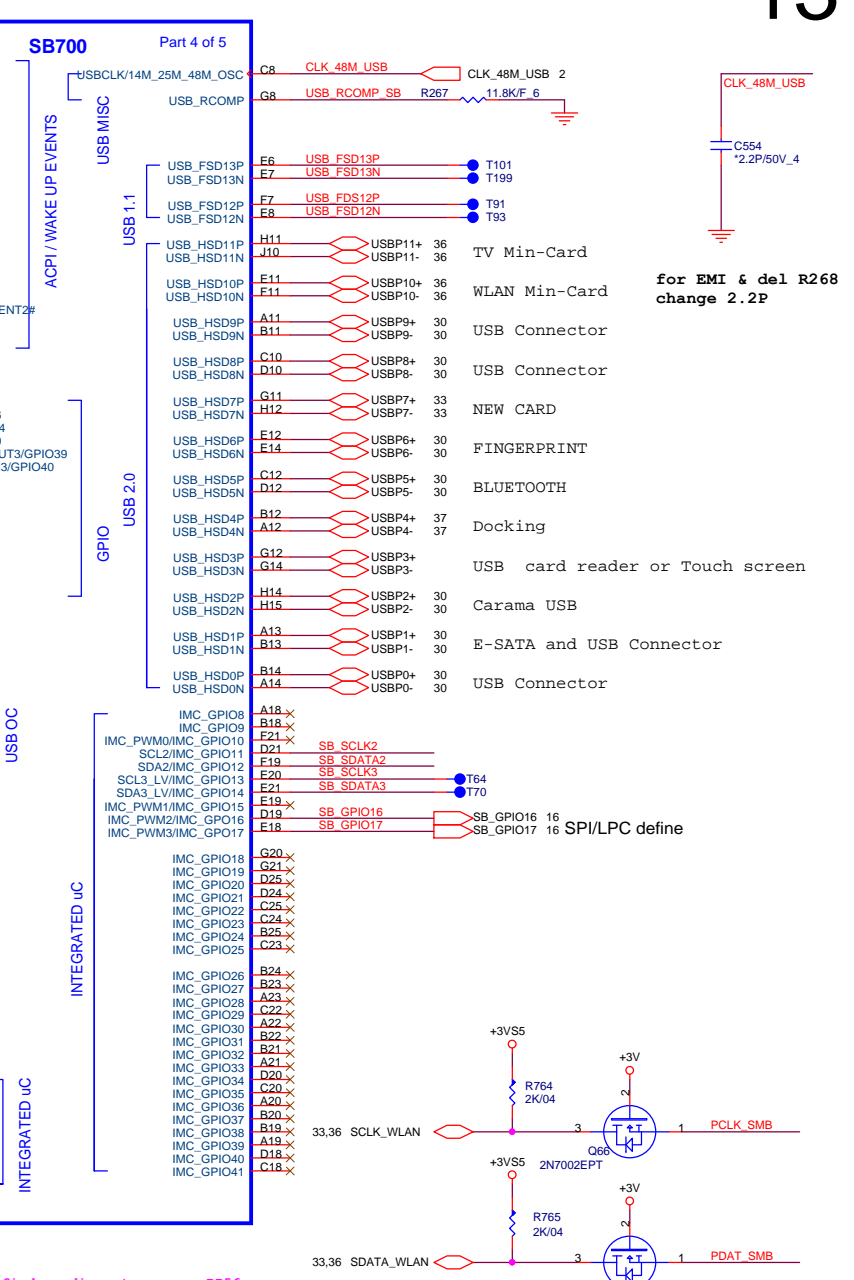
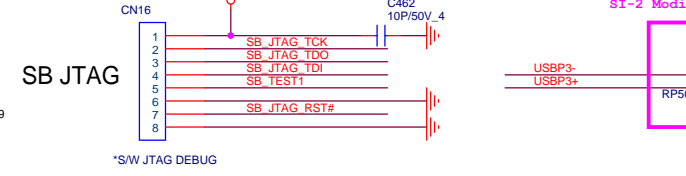
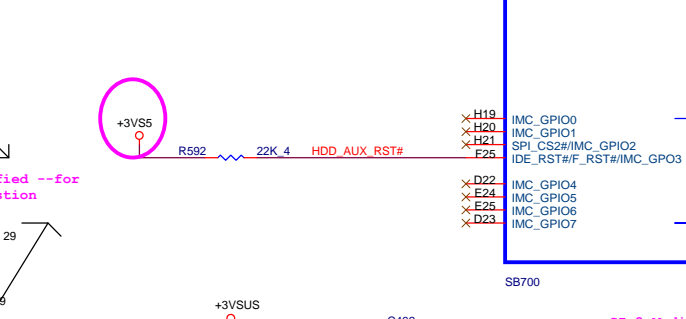
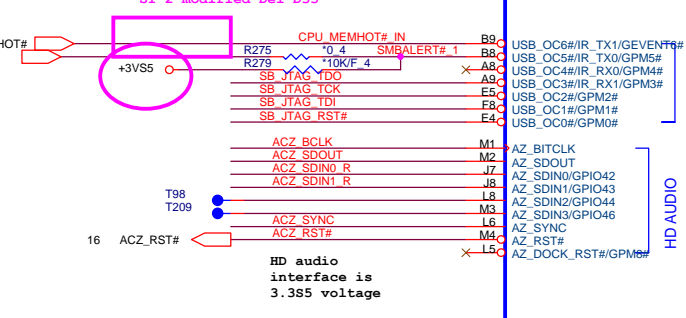
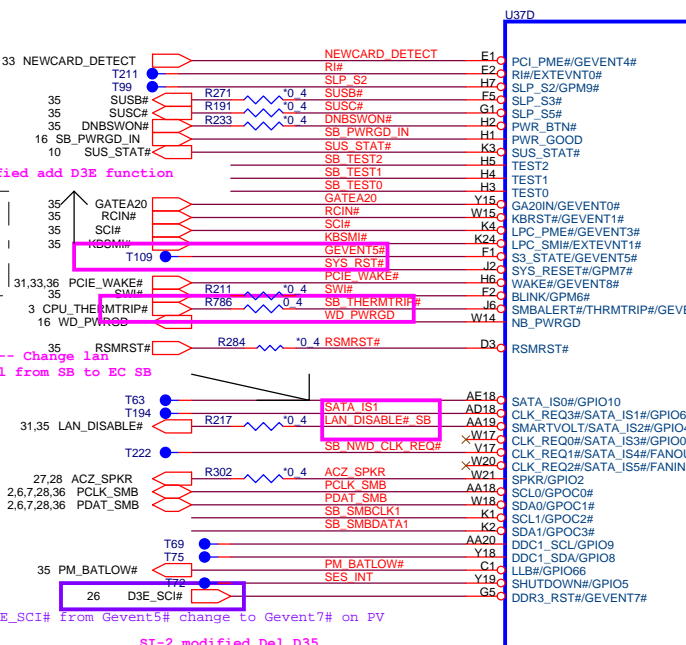
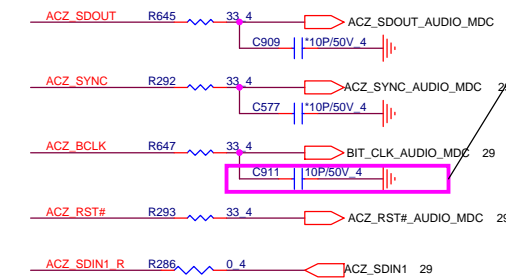




### To Azalia



### To Modem Board





SATA PORT 0,1,2,3  
can support AHCI  
mode

PLACE SATA AC COUPLING  
CAPS CLOSE TO SB600

SATA1

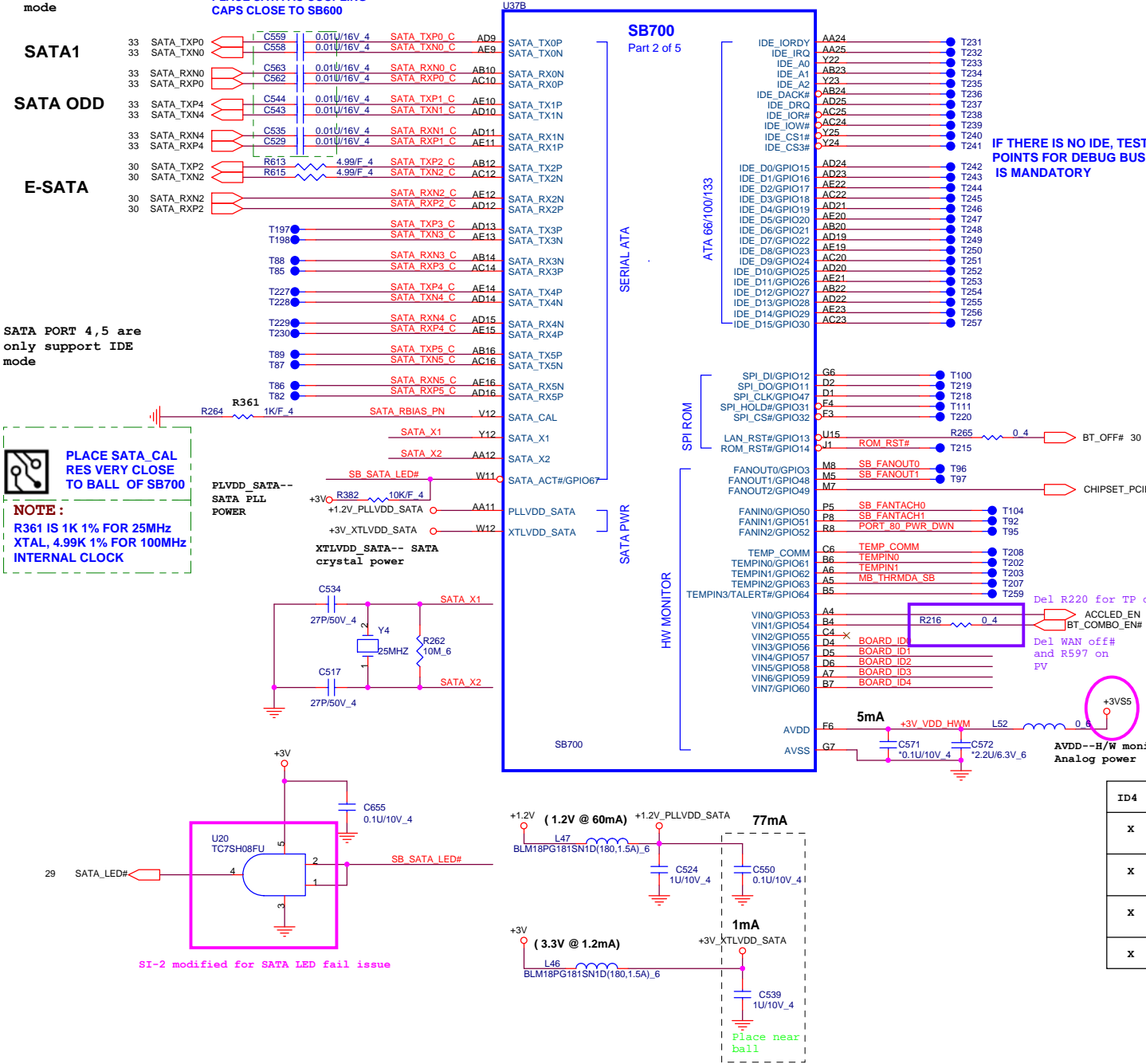
SATA ODD

E-SATA

SATA PORT 4,5 are  
only support IDE  
mode

PLACE SATA CAL  
RES VERY CLOSE  
TO BALL OF SB700

**NOTE :**  
R361 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK



IF THERE IS NO IDE, TEST  
POINTS FOR DEBUG BUS  
IS MANDATORY

SI-2 modified -- SB  
internal pull Hi to 3VS5  
, modified to same power  
rail with SB

SI-2 modified -- for fix +3V power leakage in S5 mode

ID4	ID3	ID2	ID1	ID0	
X	X	X	0	0	UMA
X	X	X	0	1	discrete
X	X	X	X	X	
X	X	X	X	X	



**PROJECT : QT8**  
Quanta Computer Inc.



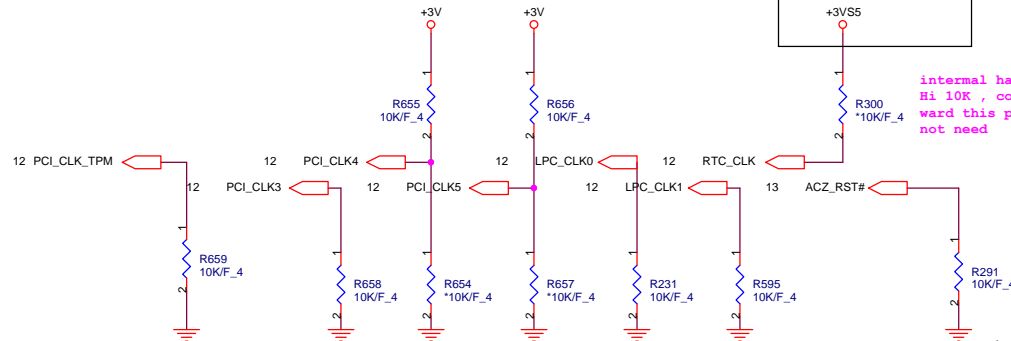


OVERLAP COMMON PADS WHERE  
POSSIBLE FOR DUAL-OP RESISTORS.

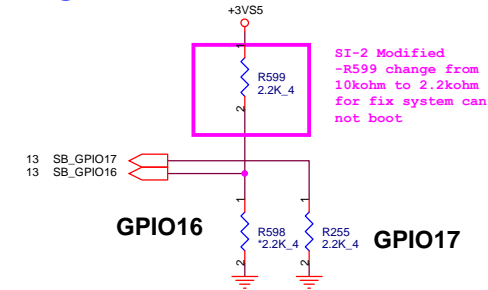
16

It must ready  
refofe RSMRST#

## REQUIRED STRAPS



	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT

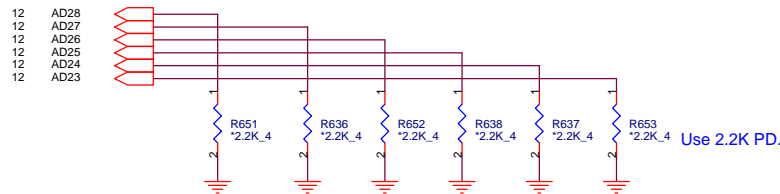


GPIO16 GPIO17

TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

## DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

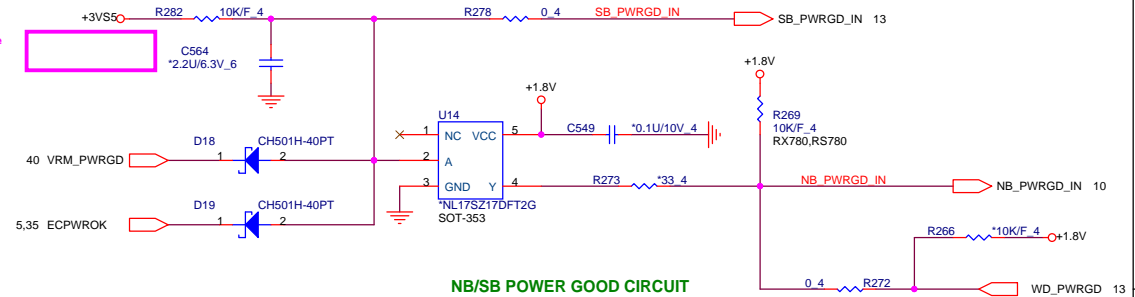


	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB\_PWRGD\_IN:  
RS780/RX780 = 1.8V; RS740 = 3.3V  
Do NOT share it with SB\_PWRGD when use Internal Clk Gen  
(Need SB PLL initialize firstly)

SI-2 modified -- confirm AMD R563 need to stuff

SI-2 modified -- remove  
+3V pull Hi resistor .



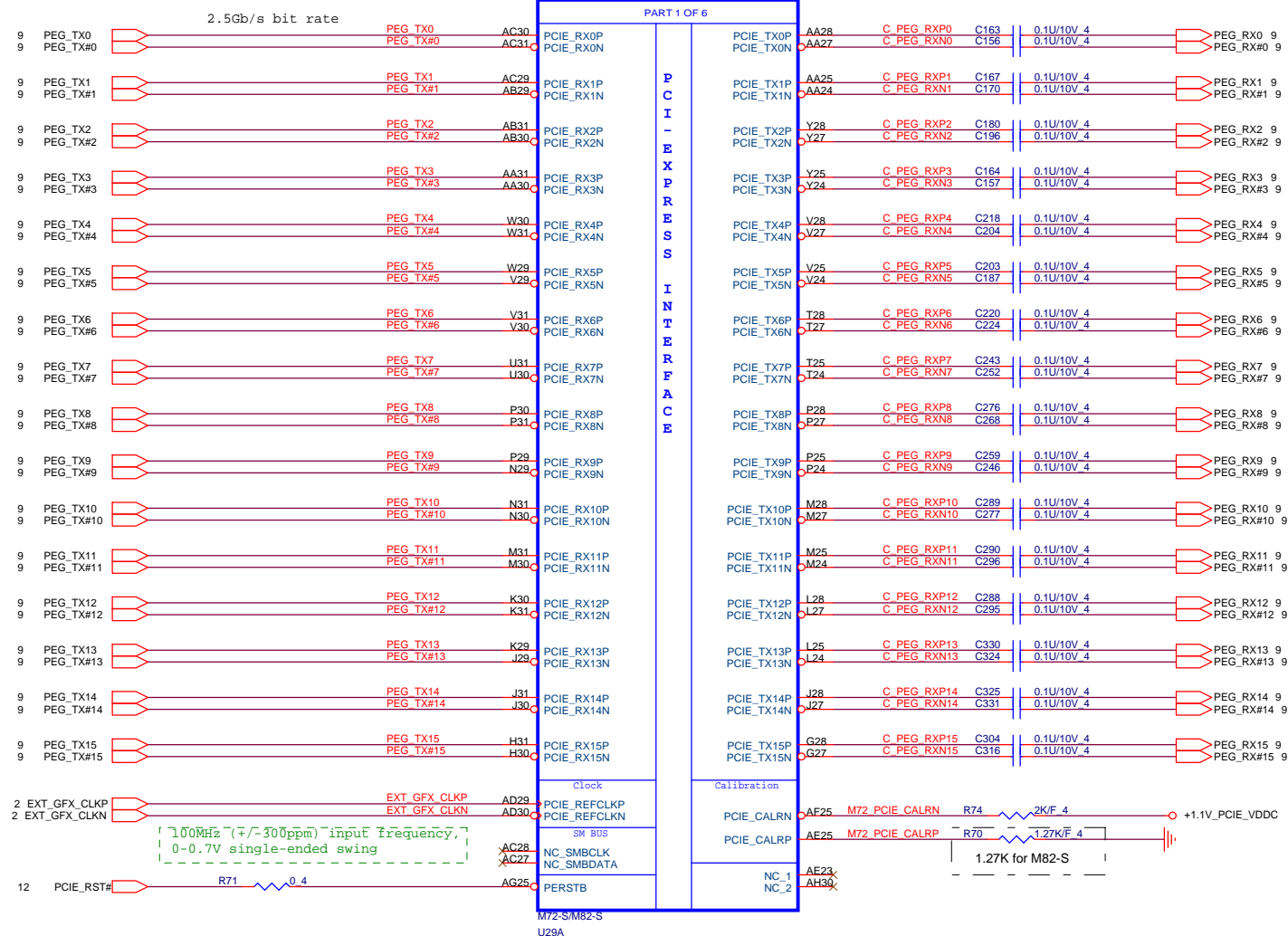
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353  
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5



PROJECT : QT8  
Quanta Computer Inc.

Size Custom Document Number  
SB700-STRAPS Rev 1A  
Date: Tuesday, February 19, 2008 Sheet 16 of 45

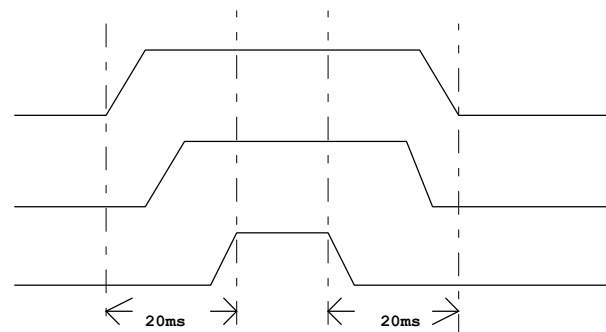
IC CTRL (632P) 216-0707001-00 (BGA)  
VGA P/N : AJ070700T00



POWER  
+PCIE\_VDDR=1.2V  
+VDD\_MEM1.8V=1.8V  
+VGA\_CORE=1.0~1.1V - M62S,M71S  
0.95~1.1V - M72S

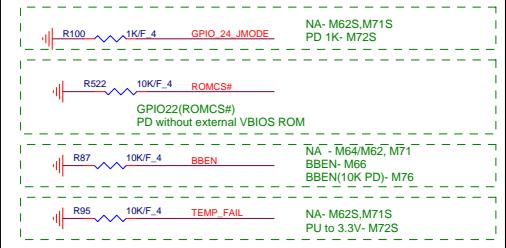
VGA Core BPP  
VGA Core VDDC  
  
+1.8V PCIE\_VDDR  
+1.8V PCIE\_PVDD  
+1.8V VDDR1

3.3V\_Delay VDDR3



**PROJECT : QT8**  
Quantia Computer Inc.

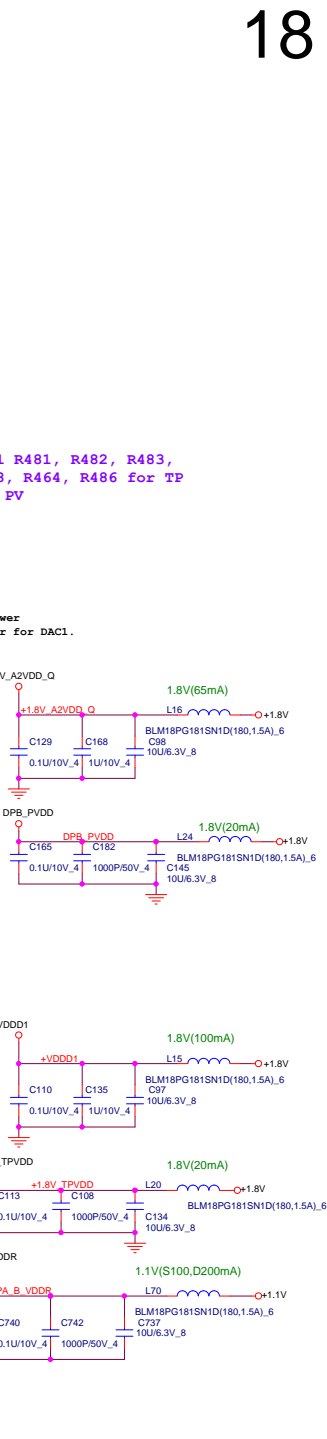
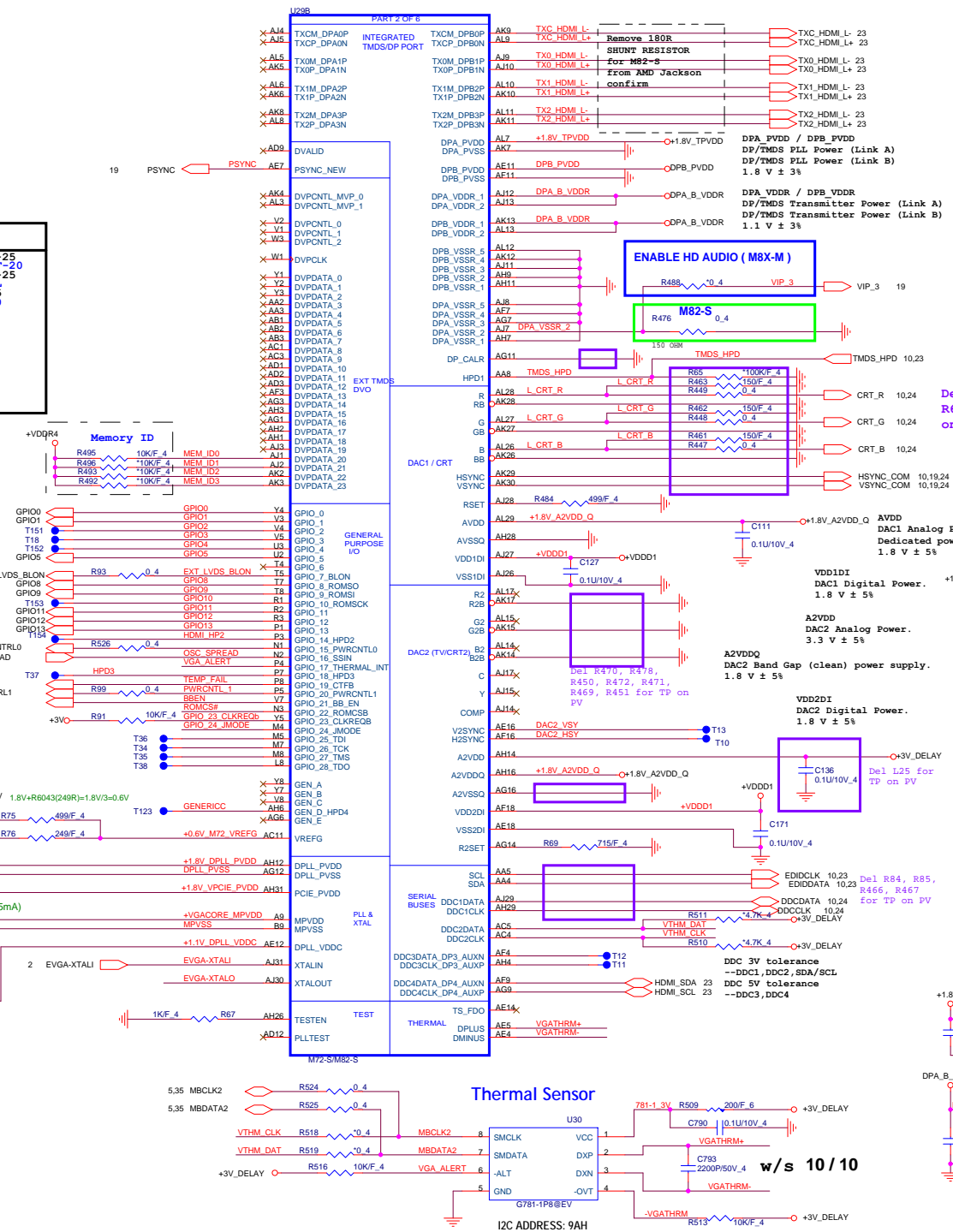
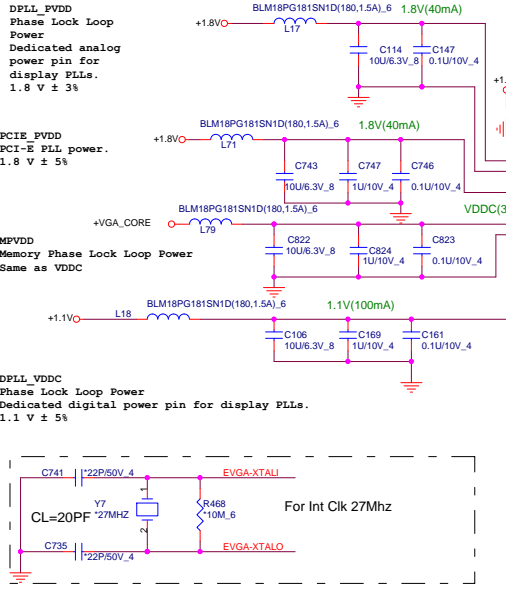
Size Custom Document Number M7X/M8X\_PCIE\_Interface Rev 1A  
Date: Tuesday, February 19, 2008 Sheet 17 of 45



MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Qimonda (Infineon)	16*16	HYB18T56161BF-25
0001	Qimonda (Infineon)	32*16-500MHZ	HYB18T512161BF-20
0010	Hynix	16*16	HY5PS561621AEP-25
0011	Hynix	32*16-500MHZ	HY5PS51621AEP-20
0100	Samsung	16*16	K4N56163QG-2C25
0101	Samsung	32*16-500MHZ	K4N51163QG-RC20
0110	Reserved		
0111	Reserved		
1000	Reserved		
1001	Reserved		
1010	Reserved		
1011	Reserved		
1100	Reserved		
1101	Reserved		
1110	Reserved		
1111	Reserved		

	PWRCNTL1	PWRCNTL0	V-CORE
H	0	0	1.1V
M	0	1	1.0V
M	1	0	1.0V
L	1	1	0.9V

	BBEN	BBP
L	0	V-CORE
H	1	+1.8V







PIN	DESCRIPTION OF DEFAULT SETTINGS	M82-S
GPIO0	PCIE FULL TX OUTPUT SWING	0
GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
GPIO5	Allows either PCIe 2.5GT/s or 5GT/s operation	REV
VIP3	ENABLE HD AUDIO ( M8X-M )	1
GPIO8	ENABLE HD AUDIO ( M82-S )	1
HSYNC	ENABLED HDMI	1

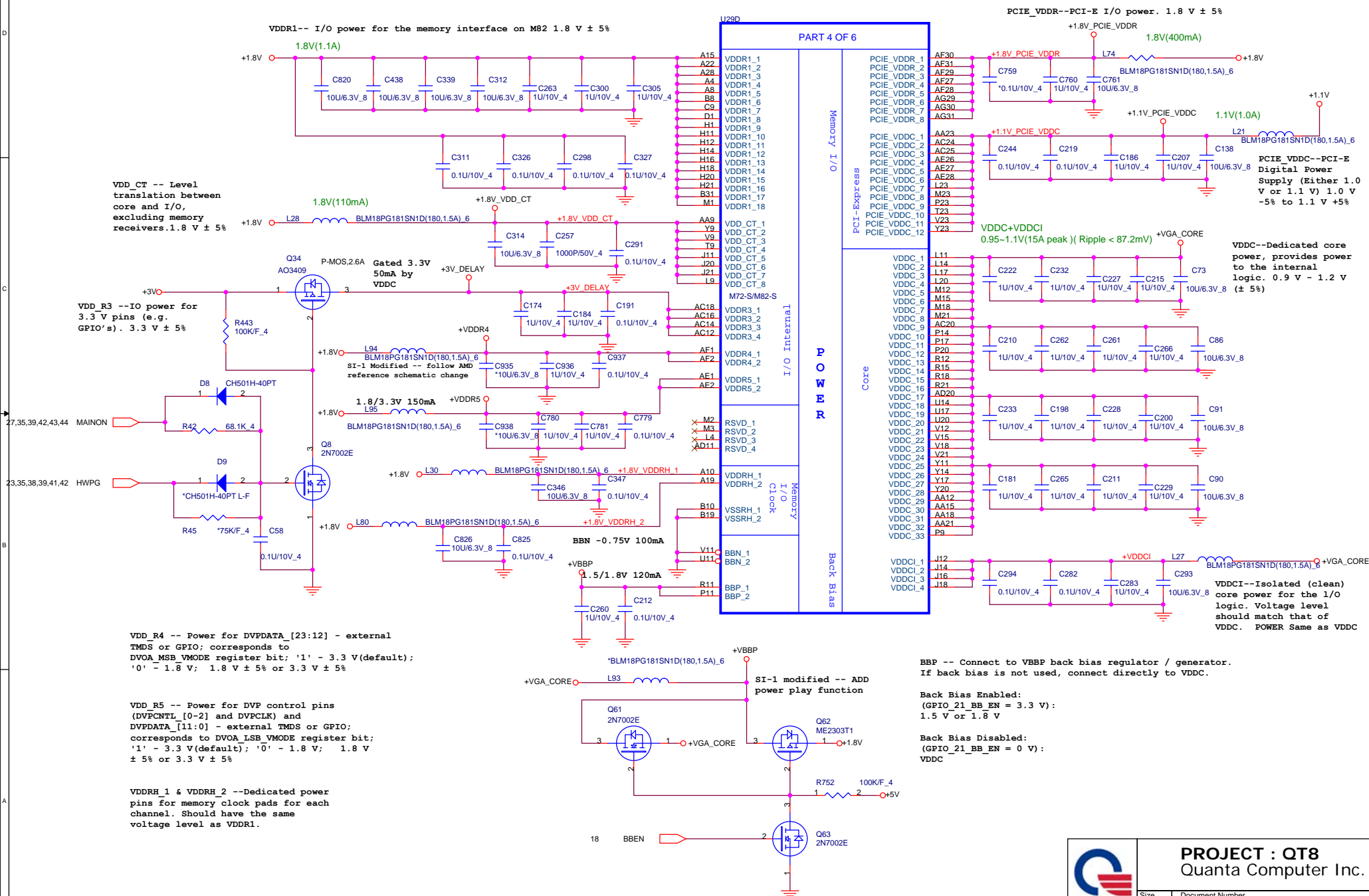
### Memory Aperture size

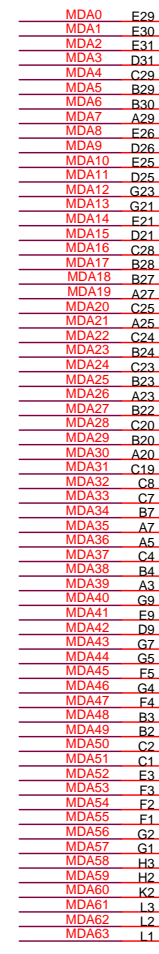
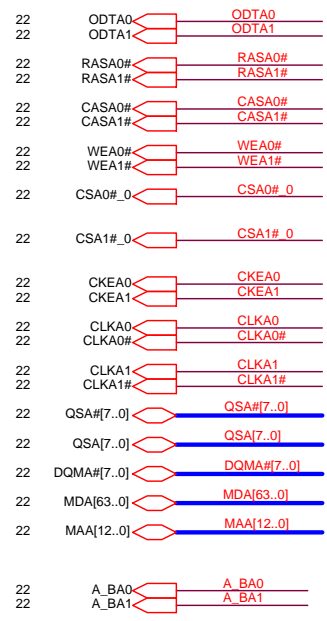
<b>GPI09</b> BIOSROM		<b>GPI013</b> ROMIDCFG2	<b>GPI012</b> ROMIDCFG1	<b>GPI011</b> ROMIDCFG0
<b>0</b>	<b>128M</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>256M</b>	<b>0</b>	<b>0</b>	<b>1</b>
<b>0</b>	<b>64M</b>	<b>0</b>	<b>1</b>	<b>0</b>
<b>0</b>	<b>32M</b>	<b>0</b>	<b>1</b>	<b>1</b>
<b>0</b>	<b>512M</b>	<b>1</b>	<b>0</b>	<b>0</b>
<b>0</b>	<b>1G</b>	<b>1</b>	<b>0</b>	<b>1</b>
<b>0</b>	<b>2G</b>	<b>1</b>	<b>1</b>	<b>0</b>
<b>0</b>	<b>4G</b>	<b>1</b>	<b>1</b>	<b>1</b>

Pin	Signal	Function	IO Type	IO Mode	IO Voltage
18	GPIO0	GPIO0	Output	*10K/F_4	
18	GPIO1	GPIO1	Output	*10K/F_4	
18	GPIO5	GPIO5	Output	*10K/F_4	
18	VIP_3	VIP_3	Output	*10K/F_4	
18	GPIO8	GPIO8	Output	*10K/F_4	
3,24	HSYNC_COM		Output	*10K/F_4	
18,24	VSYNC_COM		Output	*10K/F_4	
18	PSYNC		Output	*10K/F_4	

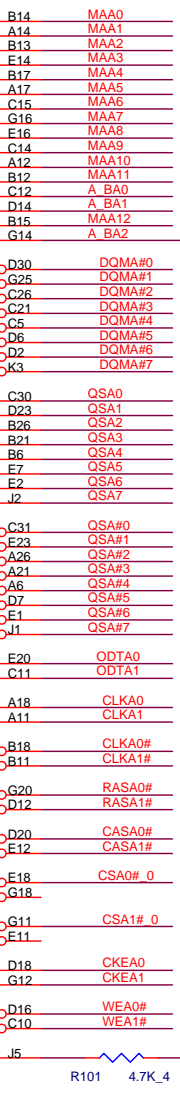
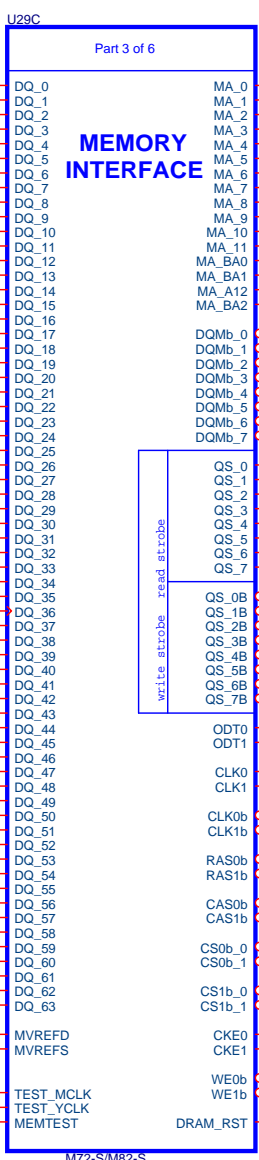
SI-1 Modified -- follow AMD  
reference schematic change for  
reduce leakage to VDDR3 BUS



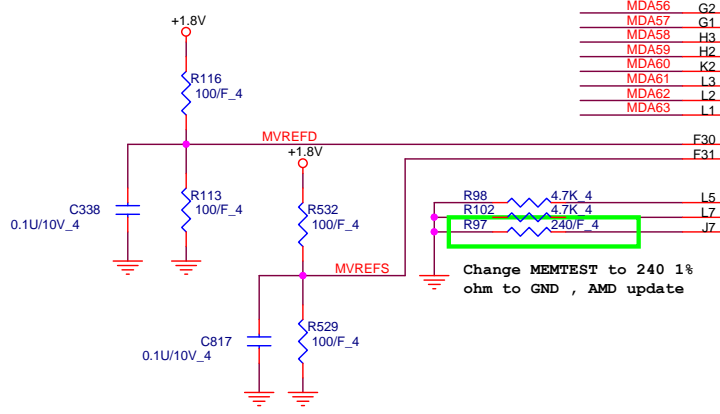





MEMORY INTERFACE



SI-1 modified --  
for support  
1Gbit VRAM ( 64M  
x 16 )

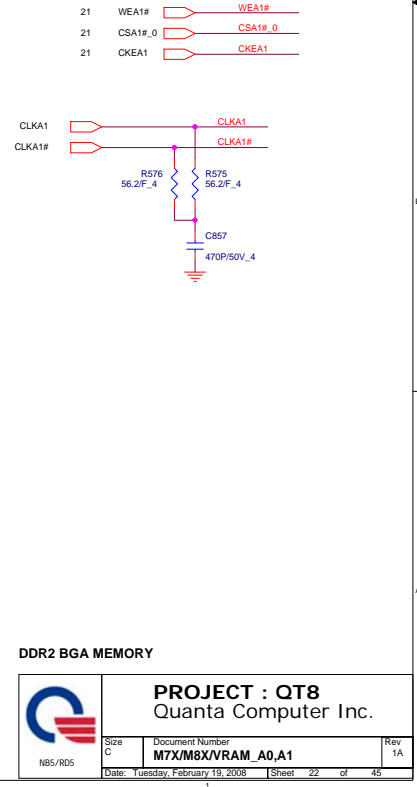
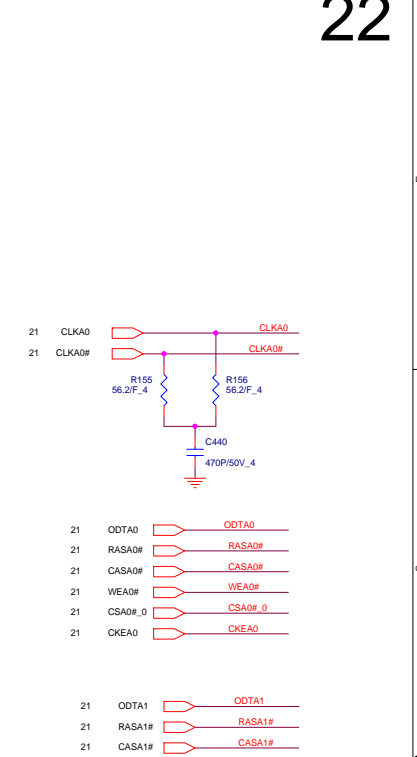


Change MEMTEST to 240 1%  
ohm to GND , AMD update

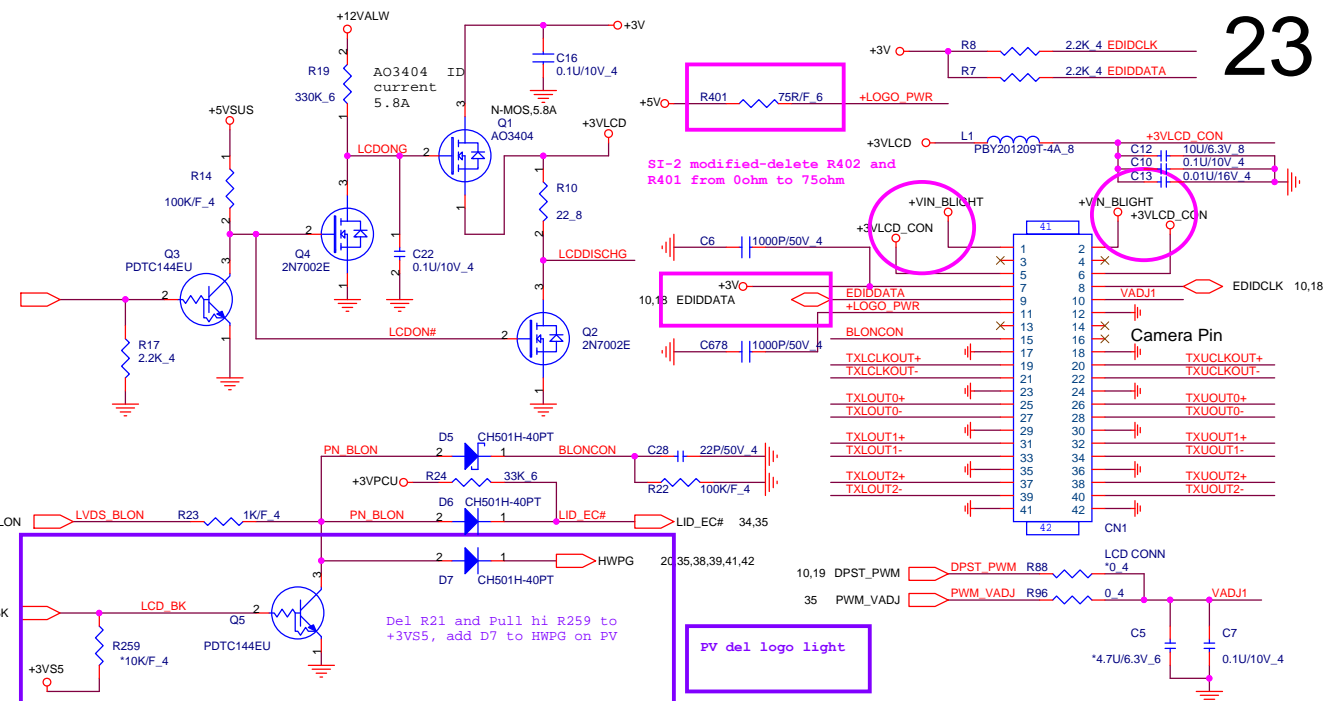
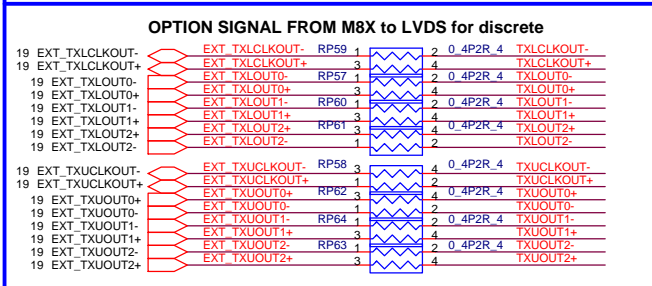
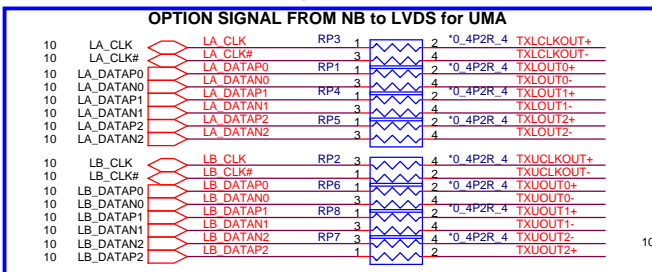


**PROJECT : QT8**  
Quanta Computer Inc.

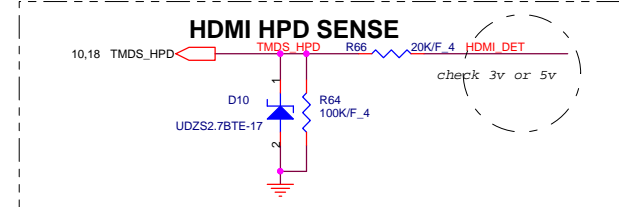
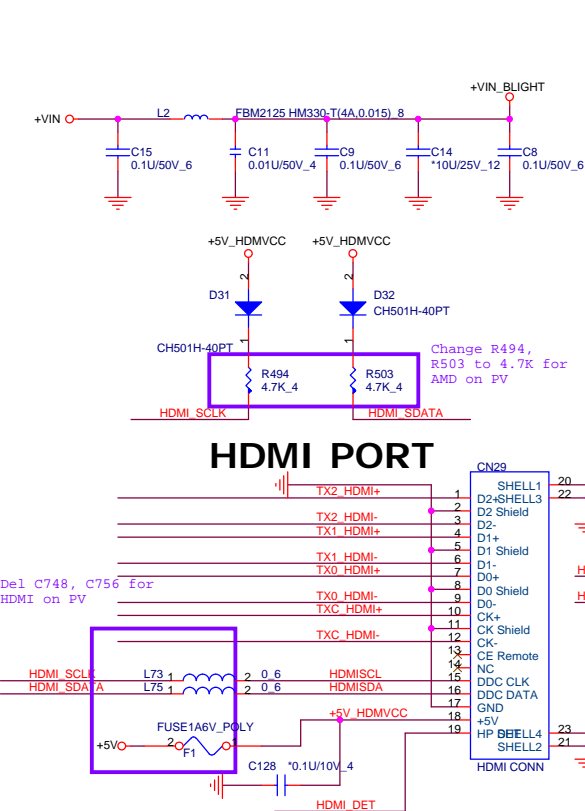
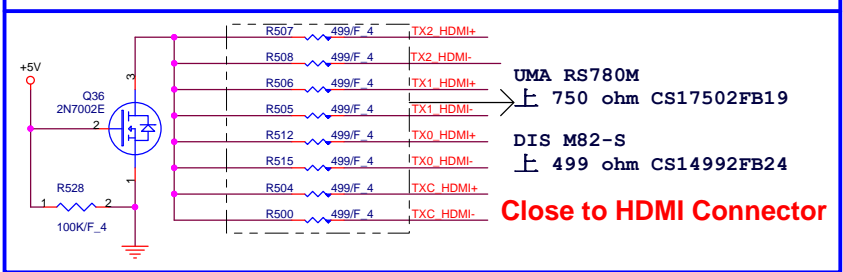
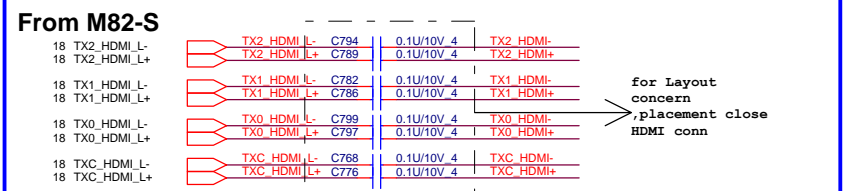
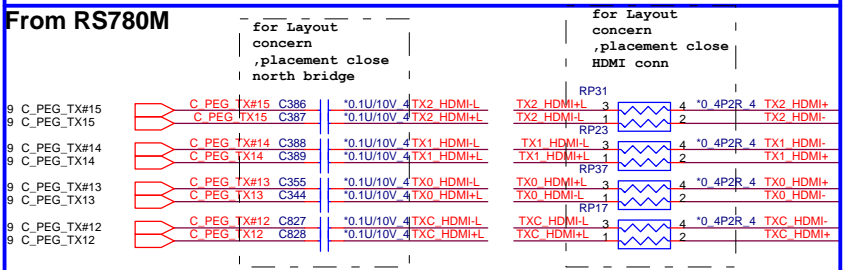
Size B	Document Number <b>M7X/M8X/MEM_Interface</b>	Rev 1A
Date: Tuesday, February 19, 2008 Sheet 21 of 45		



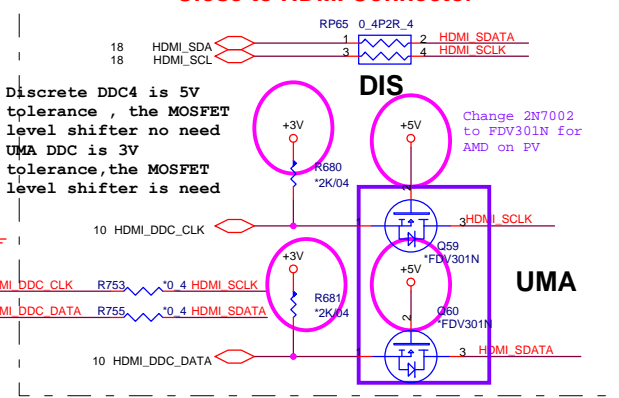
1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B



**UMA/DISCRETE select for HDMI**

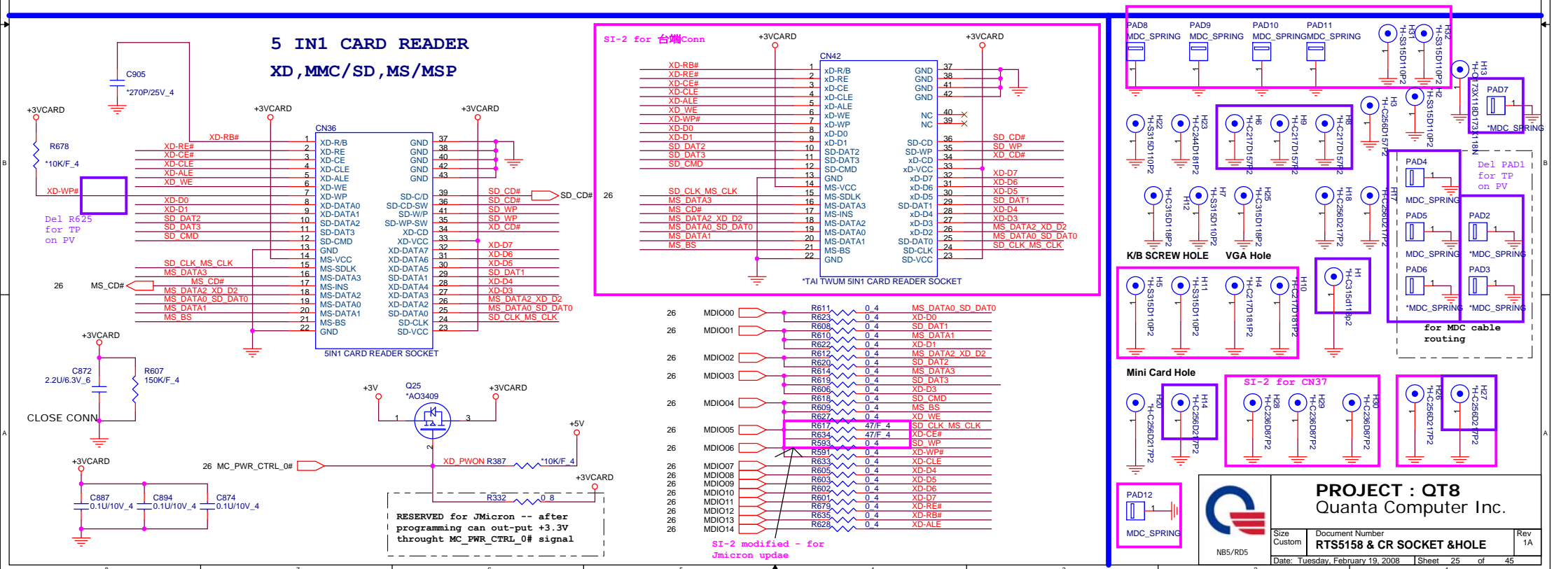
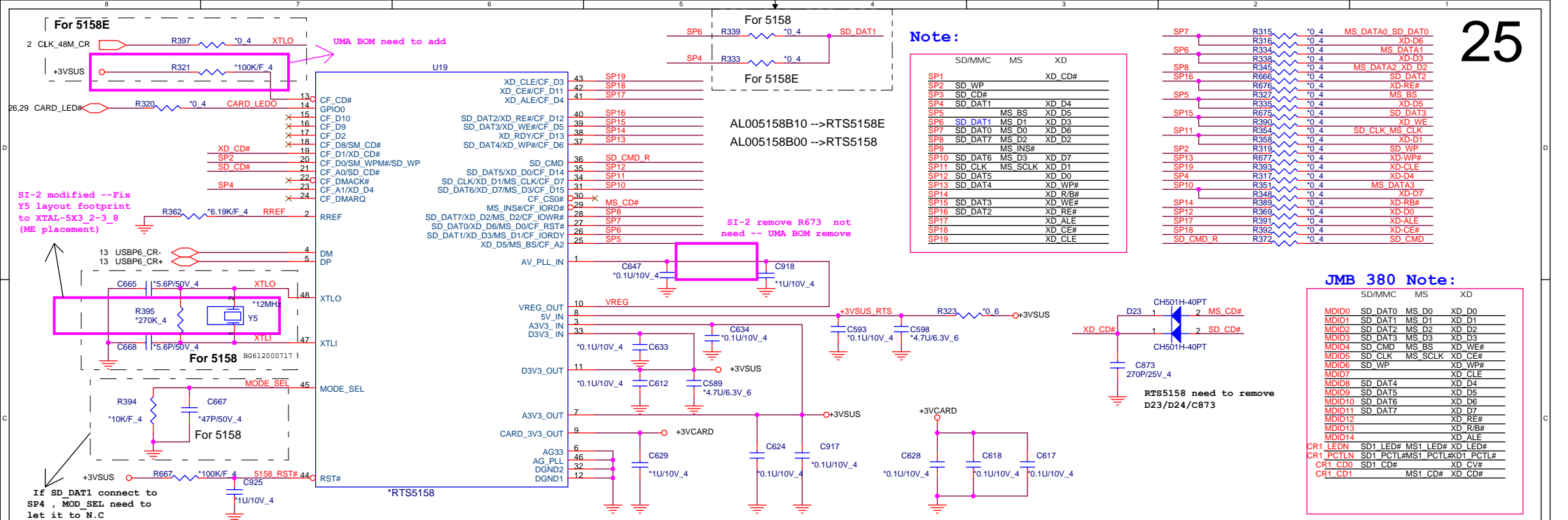


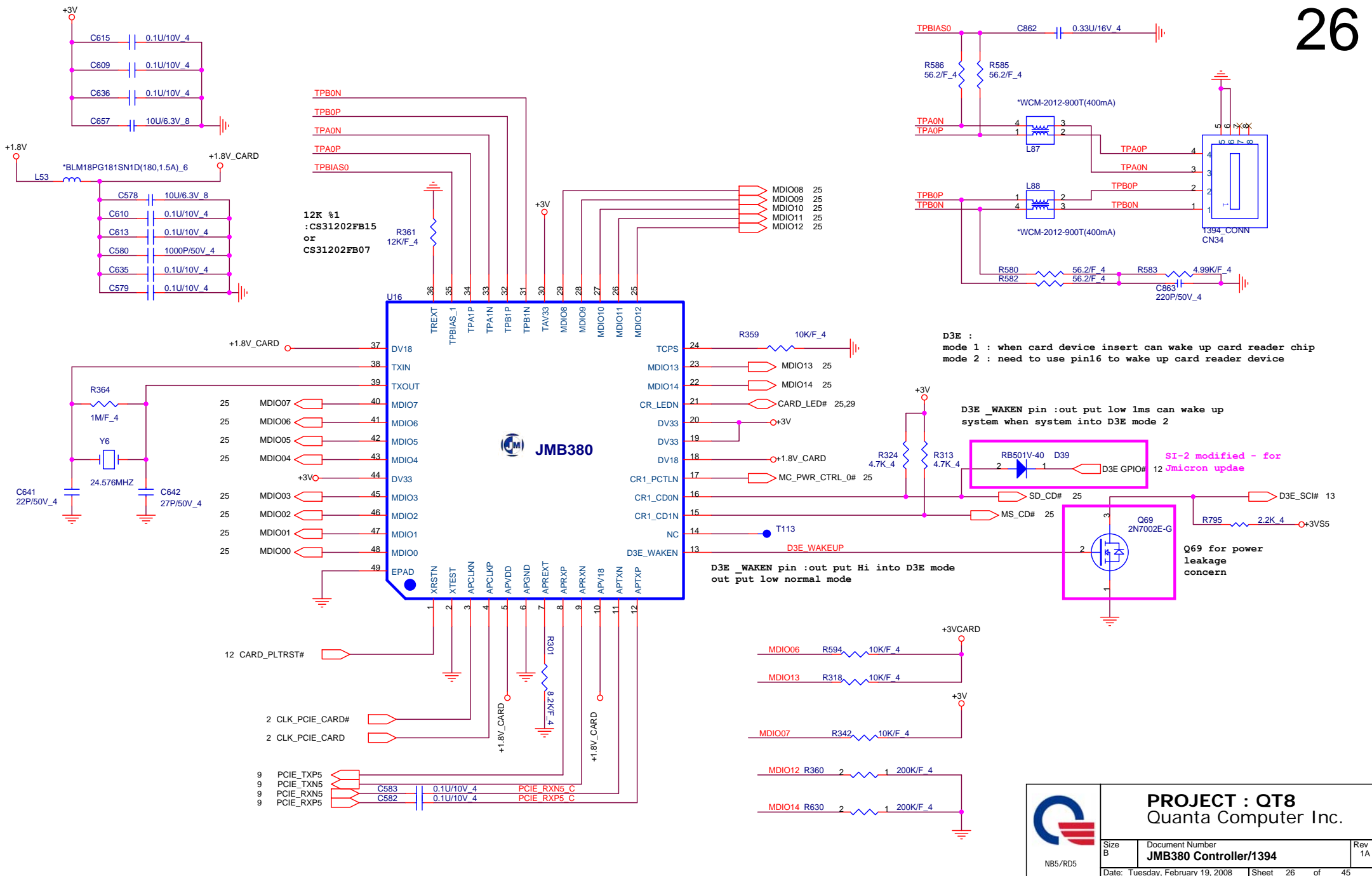
**UMA AND DISCRETE HDMI I2C SELECT**

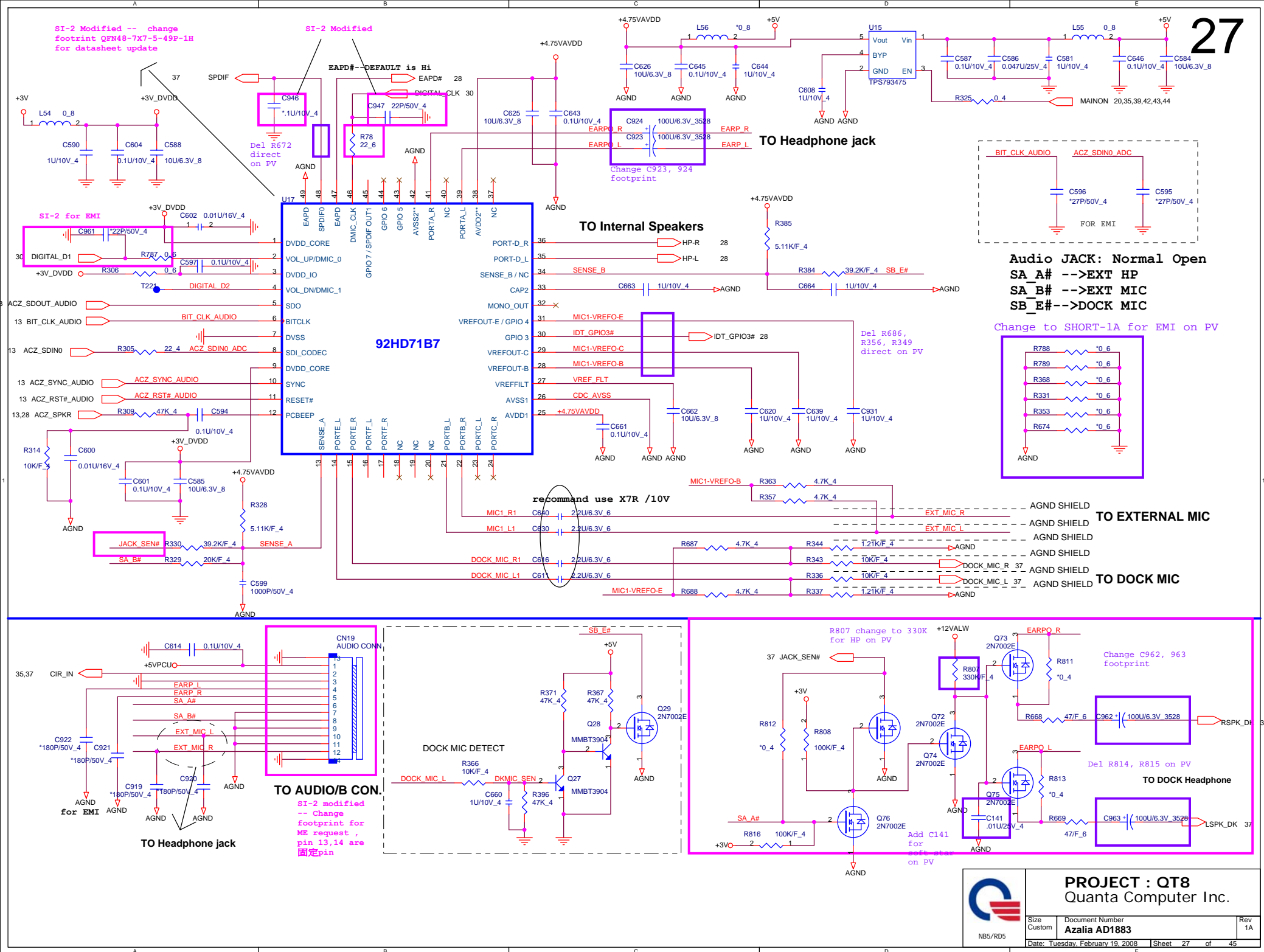




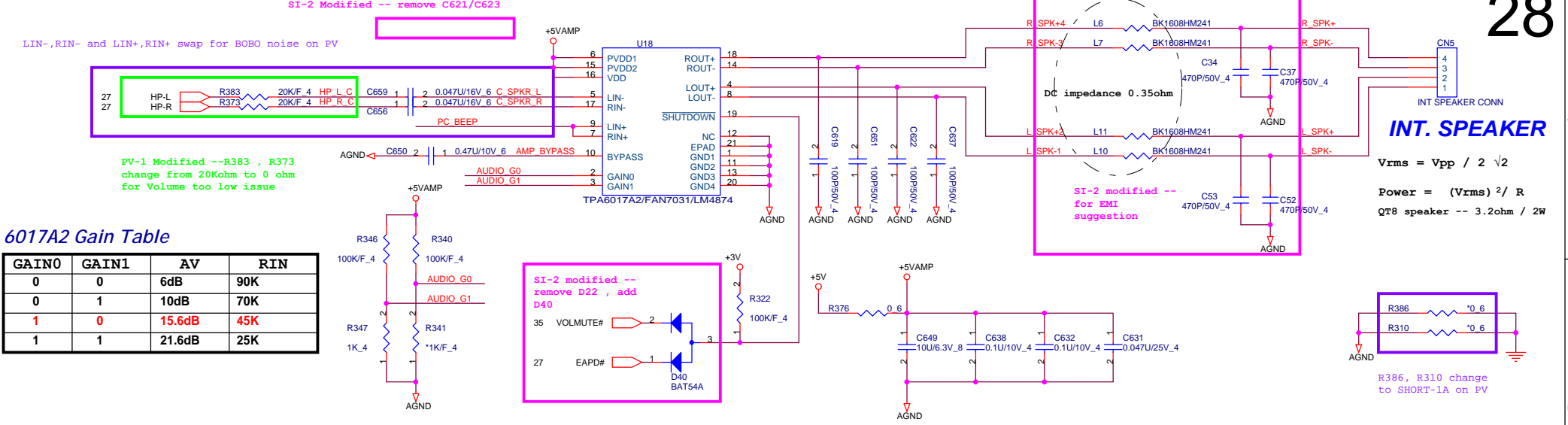




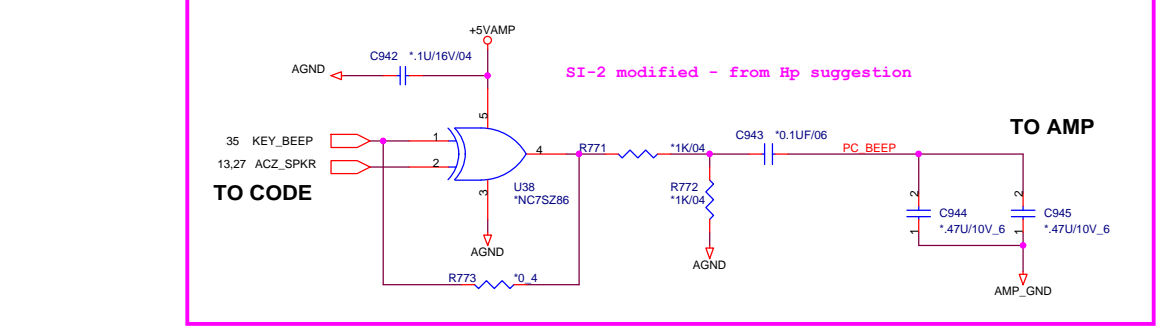




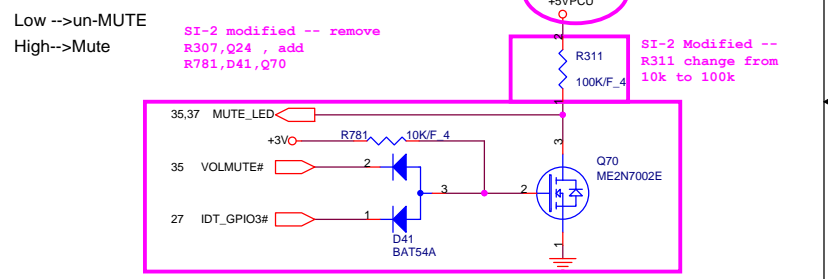
# AUDIO AMPLIFIER



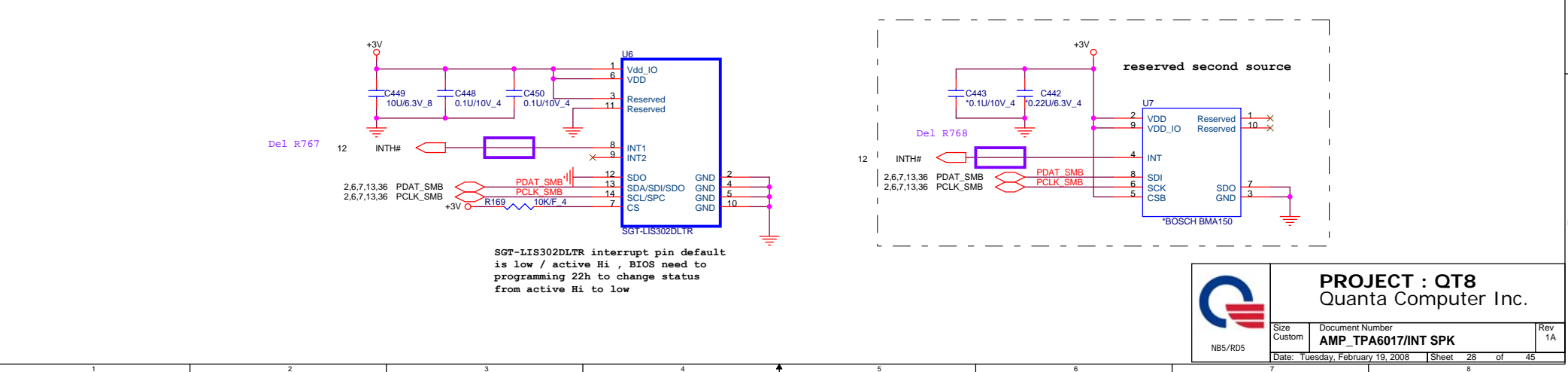
## PC-BEEP



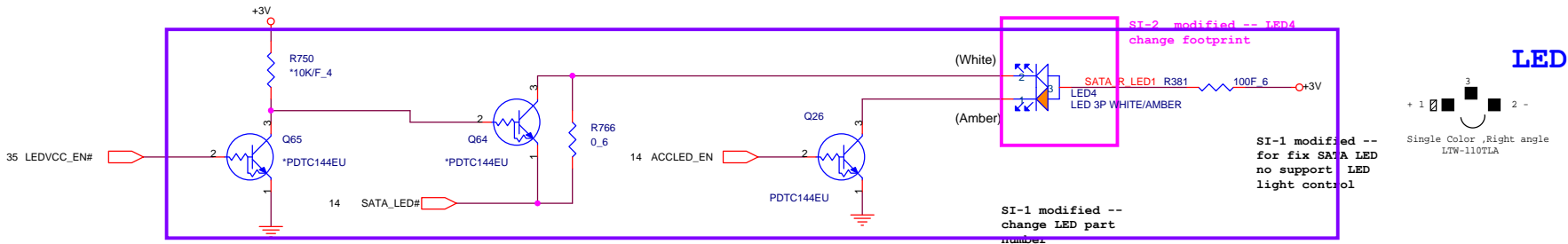
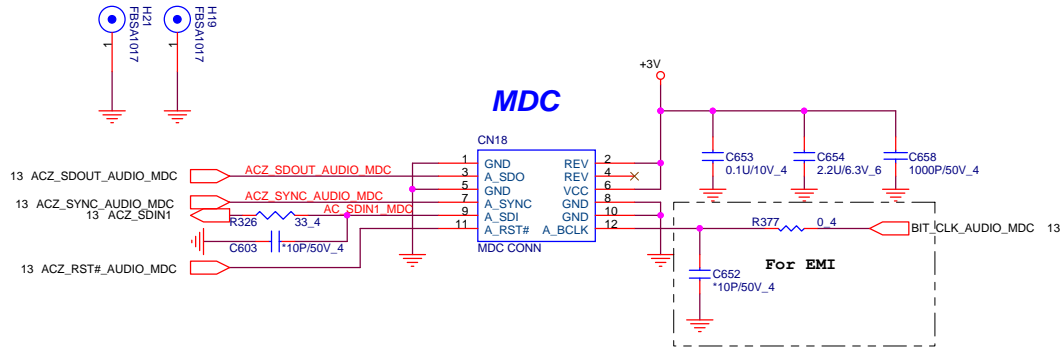
## MUTE\_LED



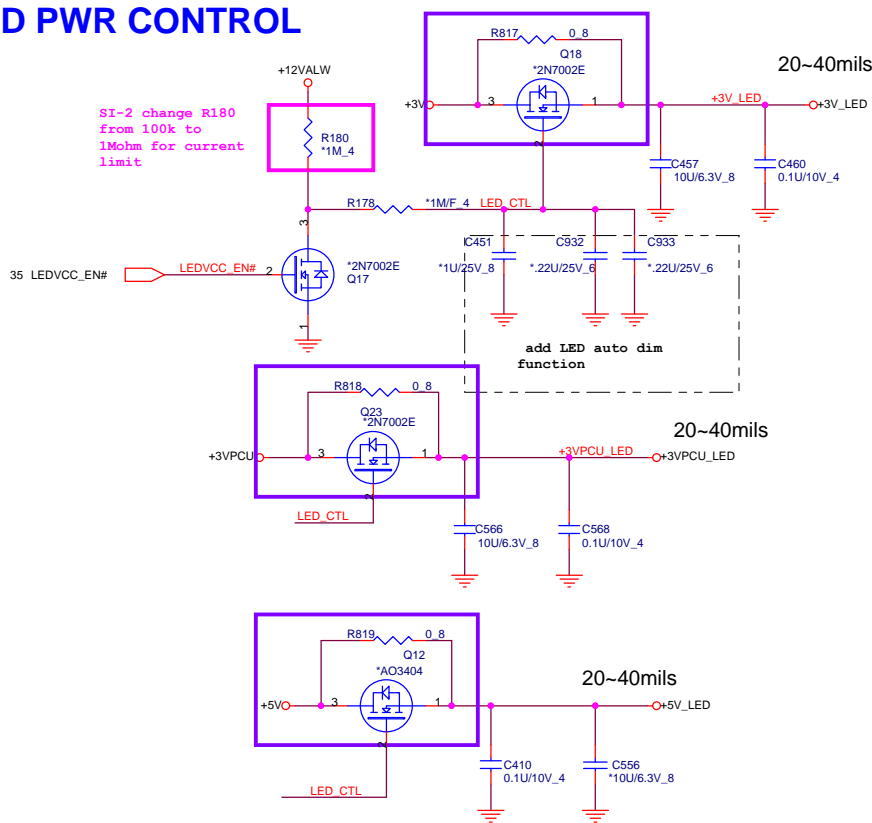
## Acceleration sensor



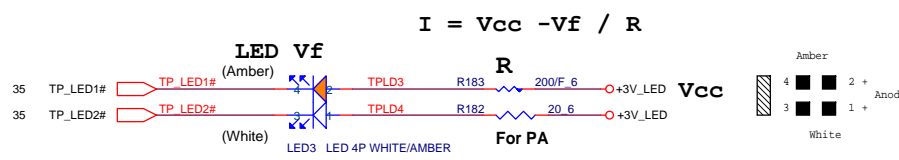
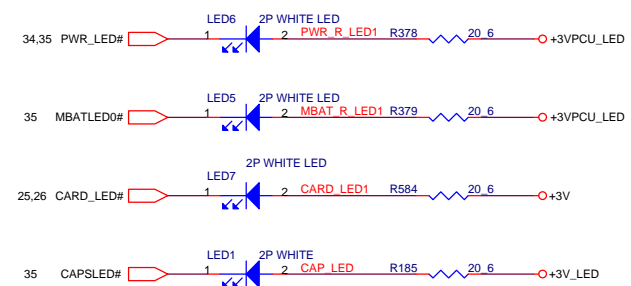




LED PWR CONTROL

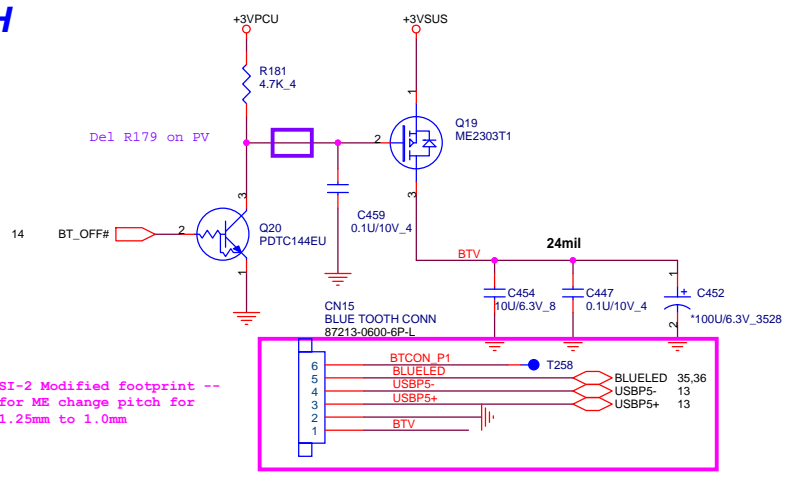


Del R380  
Change R381 to 100  
Add R766, R817, R818,  
R819  
LED PWR control no-stuff  
on PV



$$I = \frac{V_{cc} - V_f}{R}$$

BLUETOOTH

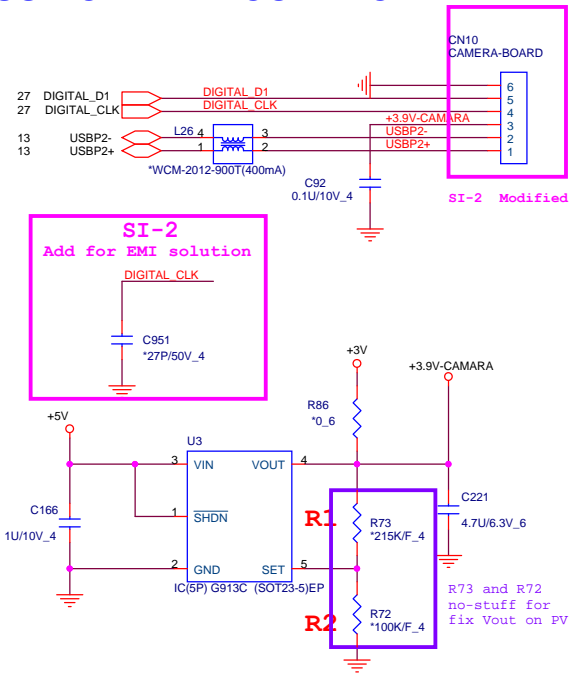


SI-2 Modified footprint --  
for ME change pitch for  
1.25mm to 1.0mm

For Discrete Touch-Screen



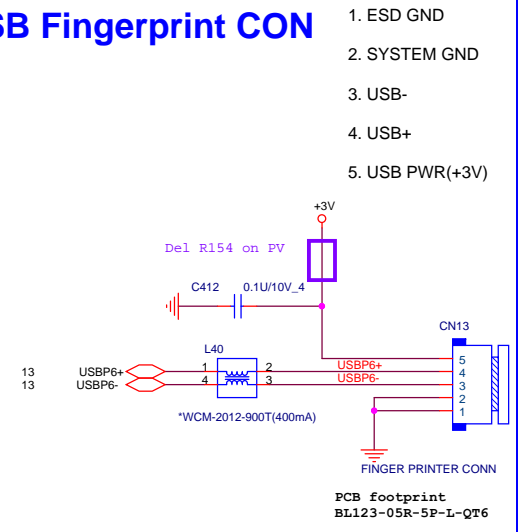
USB CAMERA CONNECT



SI-2  
Add for EMI solution  
DIGITAL\_CLK  
C951  
\*27P/50V\_4

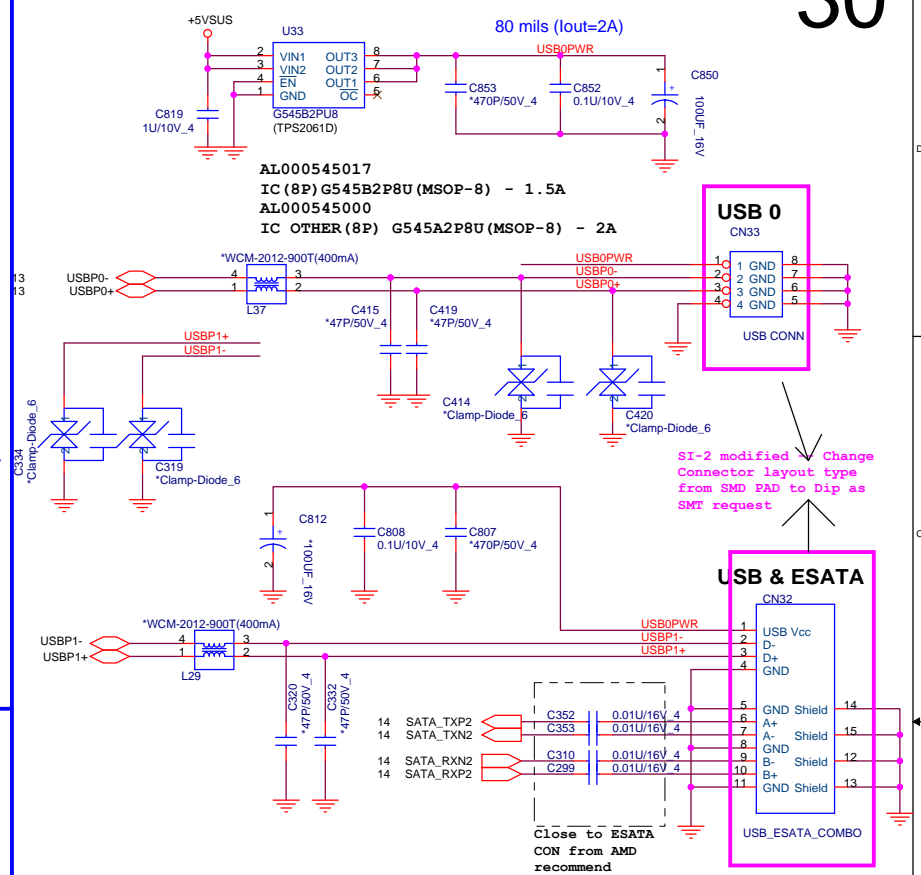
$$V_{out} = 1.25 (1 + R1/R2)$$

USB Fingerprint CON



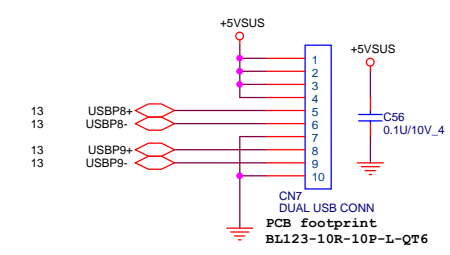
- 1. ESD GND
- 2. SYSTEM GND
- 3. USB-
- 4. USB+
- 5. USB PWR(+3V)

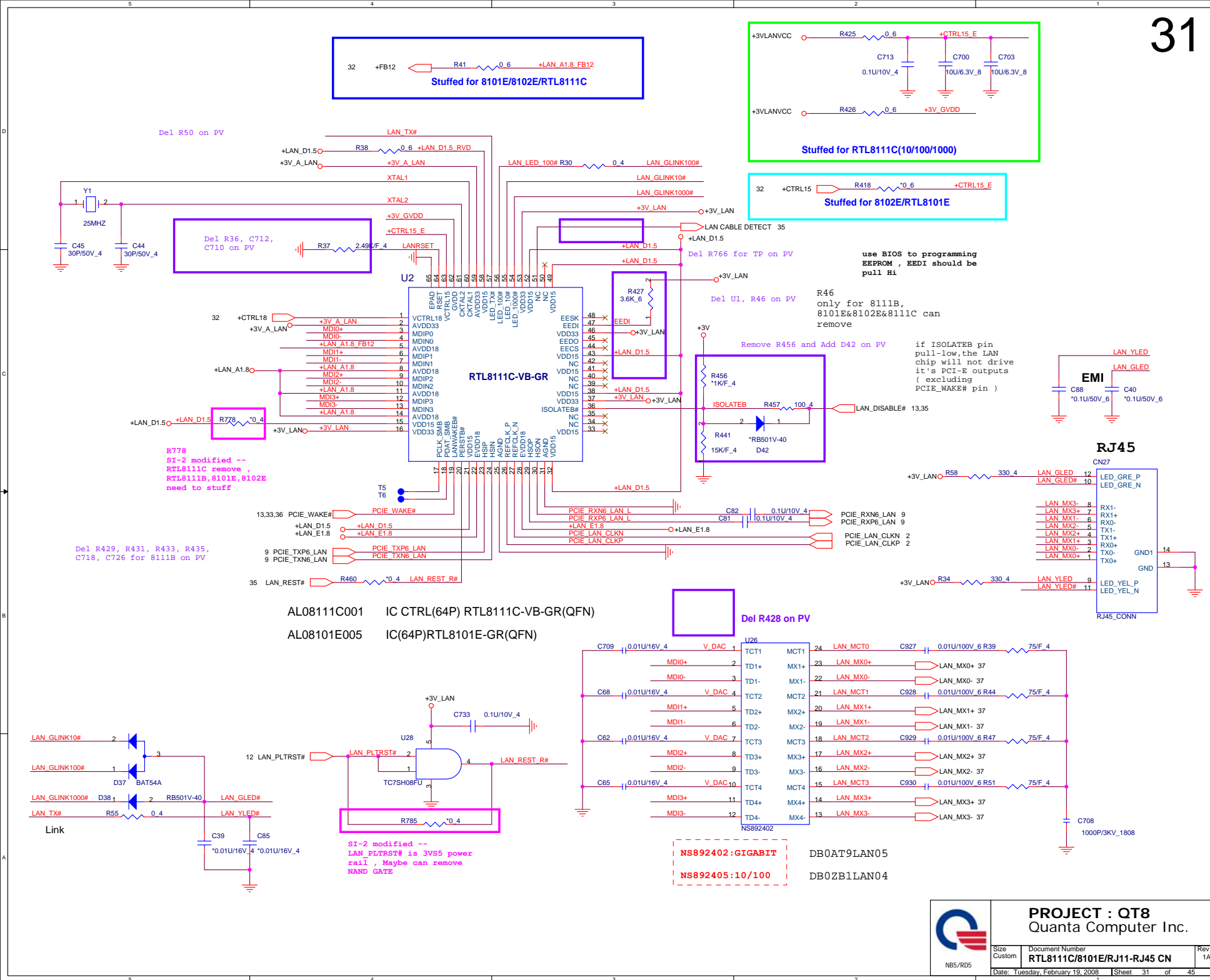
LEFT SIDE USBX1 and E-SATA/USB COMBO

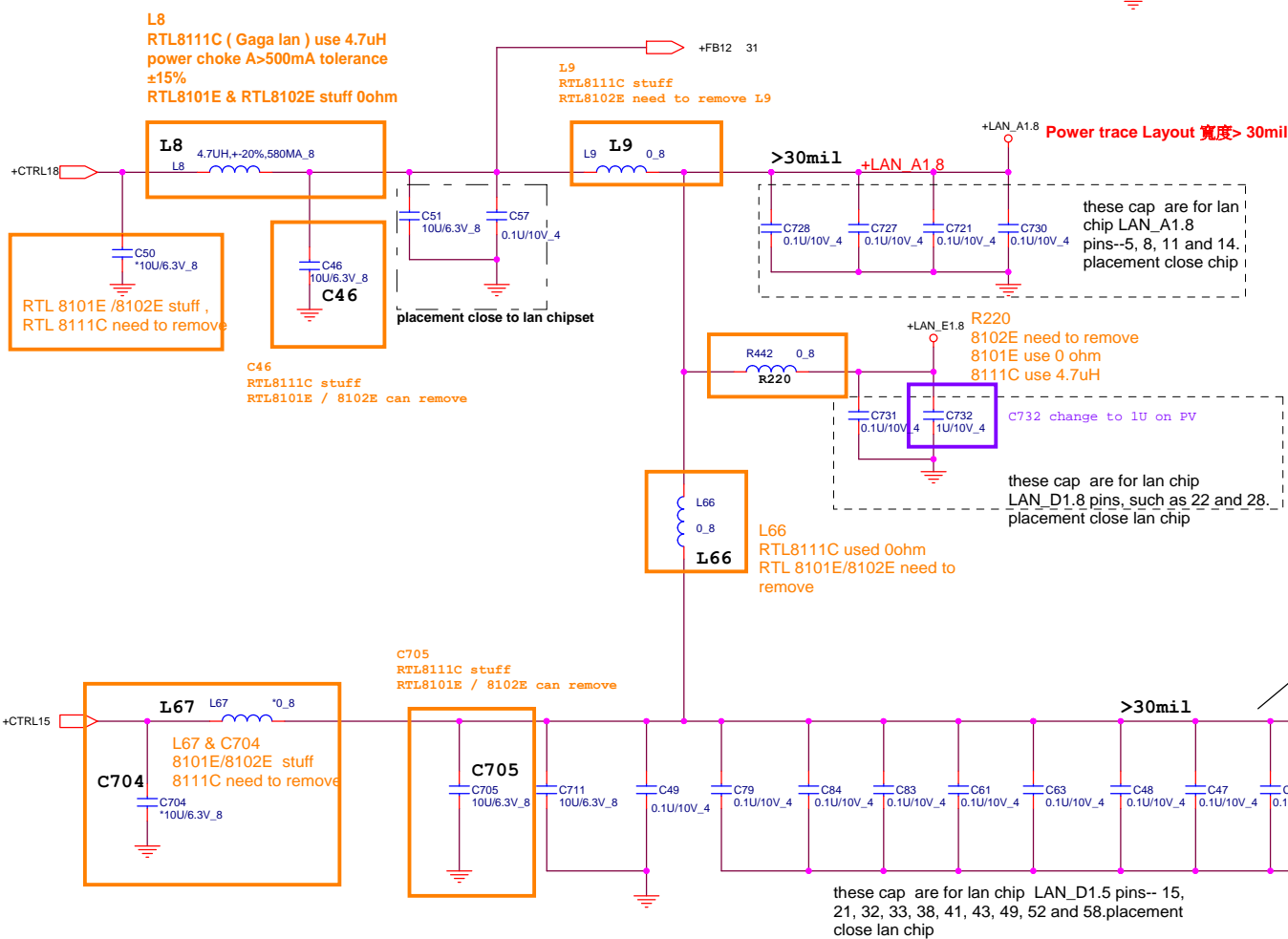
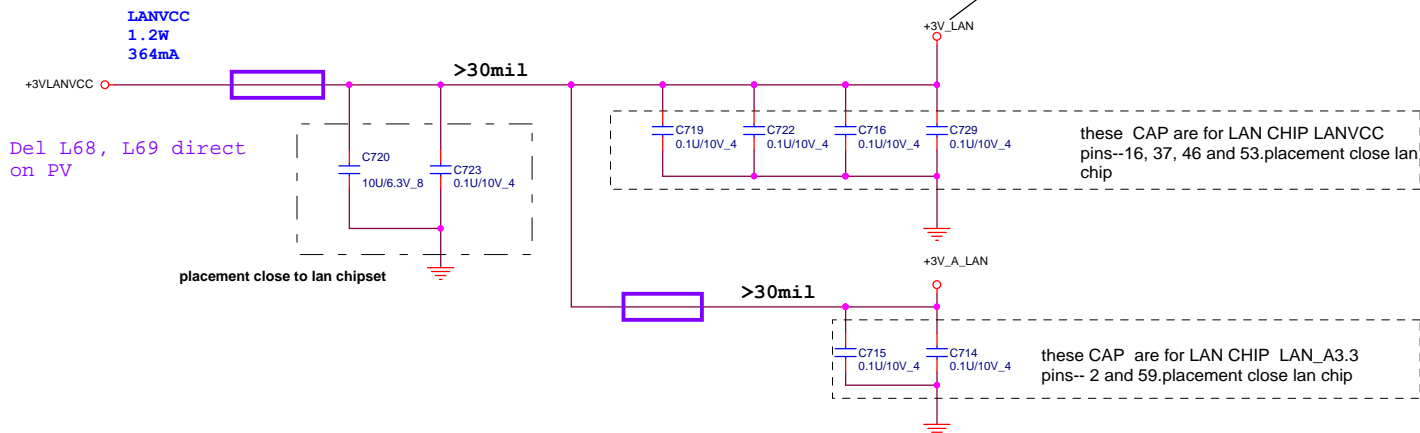


SI-2 modified -- Change  
Connector layout type  
from SMD PAD to Dip as  
SMT request

RIGHT SIDE USBX2







Power domain chart

	RTL8111B / RTL8101E	RTL8111C RTL8102E
LANVCC	3.3V	3.3V
LAN_D1.8	1.8V	1.2V
LAN_A1.8	1.8V	1.2V
LAN_D1.5	1.5V	1.2V



NBS/RD5

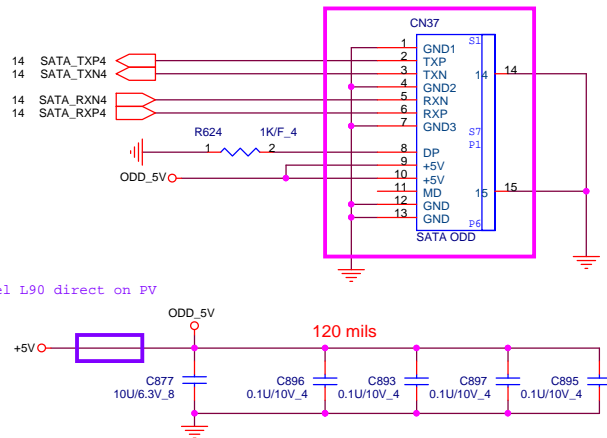
**PROJECT : QT8**  
Quanta Computer Inc.

Size  
CustomDocument Number  
**LAN Power**Rev  
1A

Date: Tuesday, February 19, 2008 Sheet 32 of 45

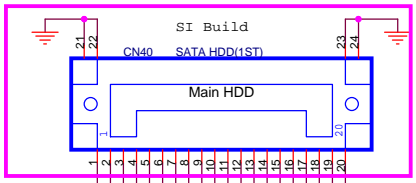
# SATA CD-ROM

SI-2 Modified footprint -- Modify 12/27



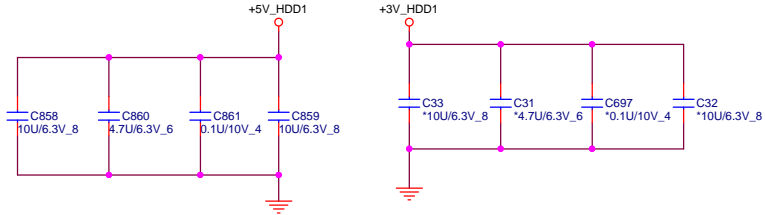
Del L90 direct on PV

SI-2 Modified footprint -- Modify 固定孔 Size as SMT request



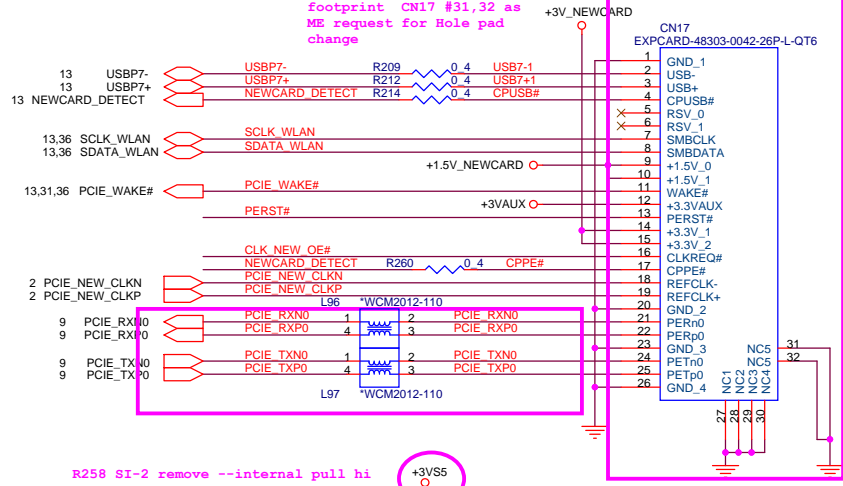
+5V: 2 A(4 Pin)  
+3V: 2 A(4 Pin)  
Gnd: (5 Pin)

Del R578 direct on PV

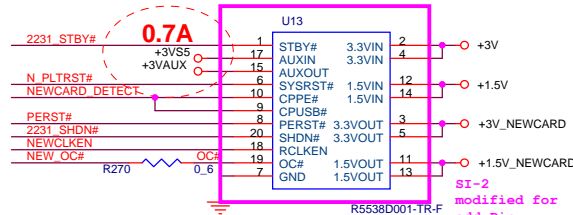
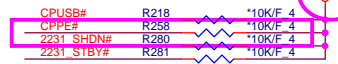


# NEWCARD

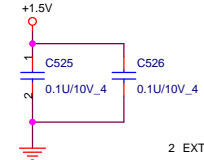
SI-1 modified -- change footprint CN17 #31,32 as ME request for Hole pad change



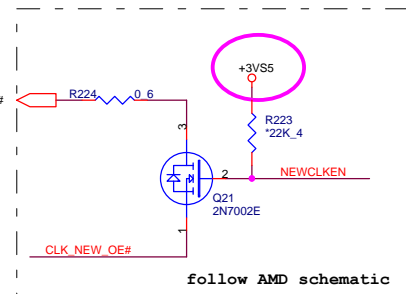
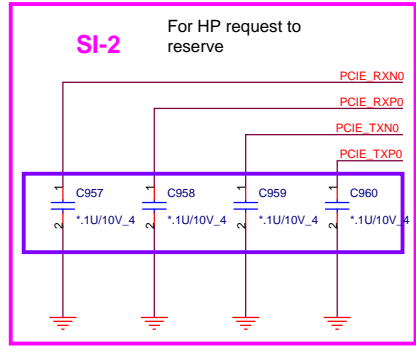
R258 SI-2 remove --internal pull hi



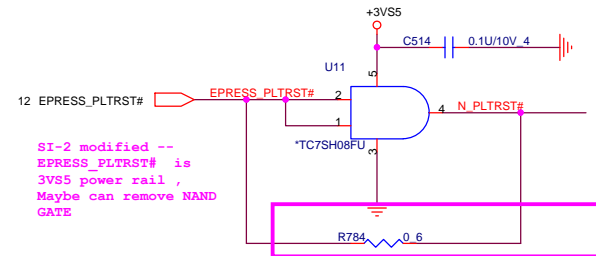
R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN




Del R790, R791, R792, R793 for RF on PV



follow AMD schematic



SI-2 modified -- EPRESS\_PLTRST# is 3VS5 power rail, Maybe can remove NAND GATE



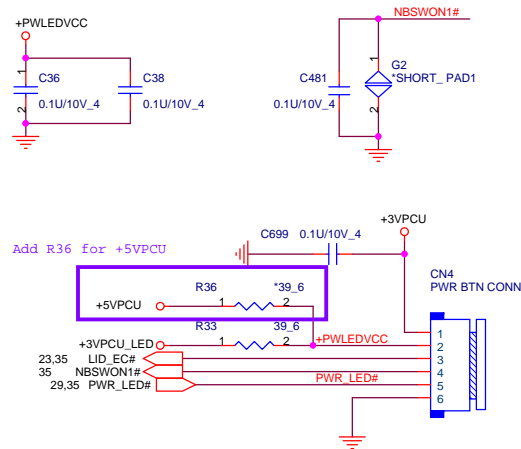
PROJECT : QT8

Quanta Computer Inc.

Size Custom	Document Number NEW CARD/SATA ODD/SATA HDD	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 33	of 45

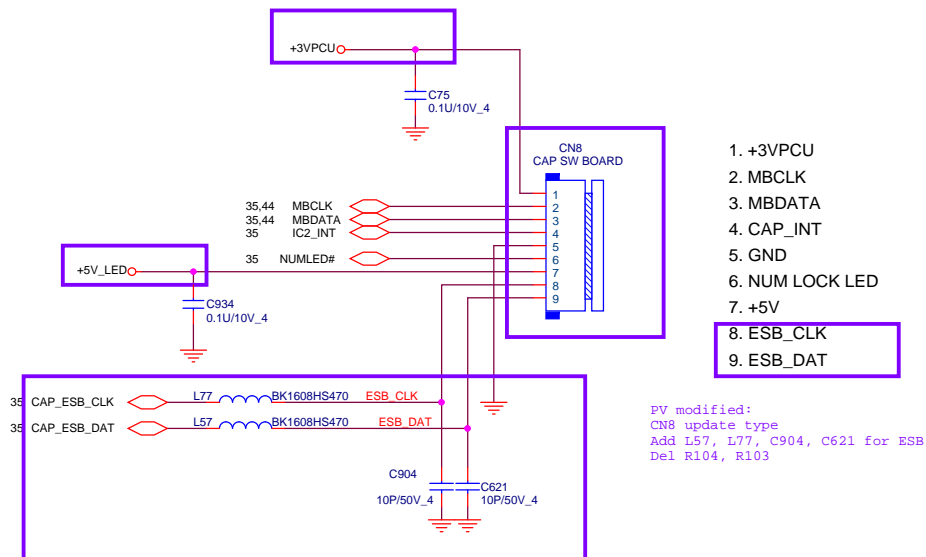


## POWER BUTTON CONNECT



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

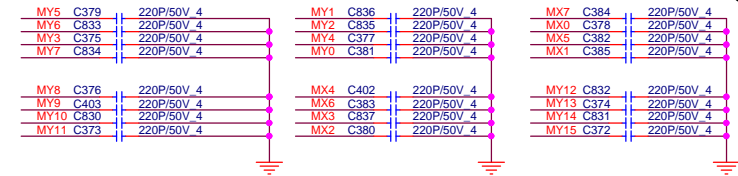
## CAP SW CONNECT



1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP\_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB\_CLK
9. ESB\_DAT

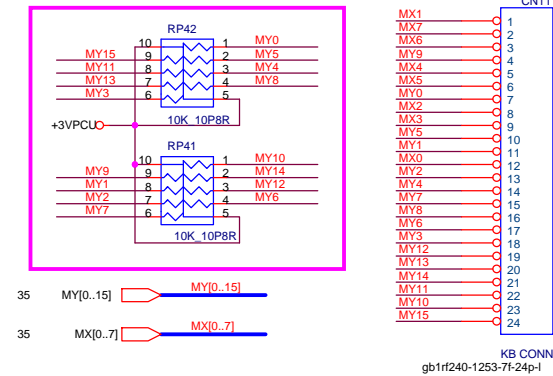
PV modified:  
CN8 update type  
Add L57, L77, C904, C621 for ESB  
Del R104, R103

34



SI-2 Modified  
-- net swap for  
layout concern

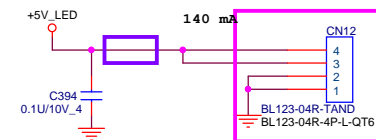
## KEYBOARD PULL-UP



KB CONN  
gb1rf240-1253-7f-24p-l

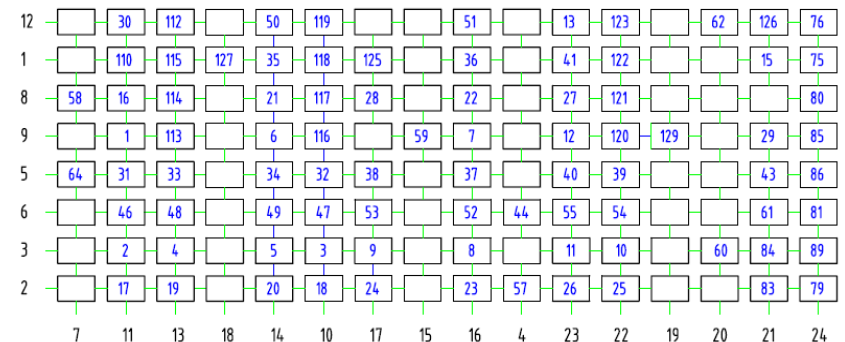
Del R770 on PV

SI-2 Modified 12/27



1. LEDVCC
2. LEDVCC
3. NC
4. GND

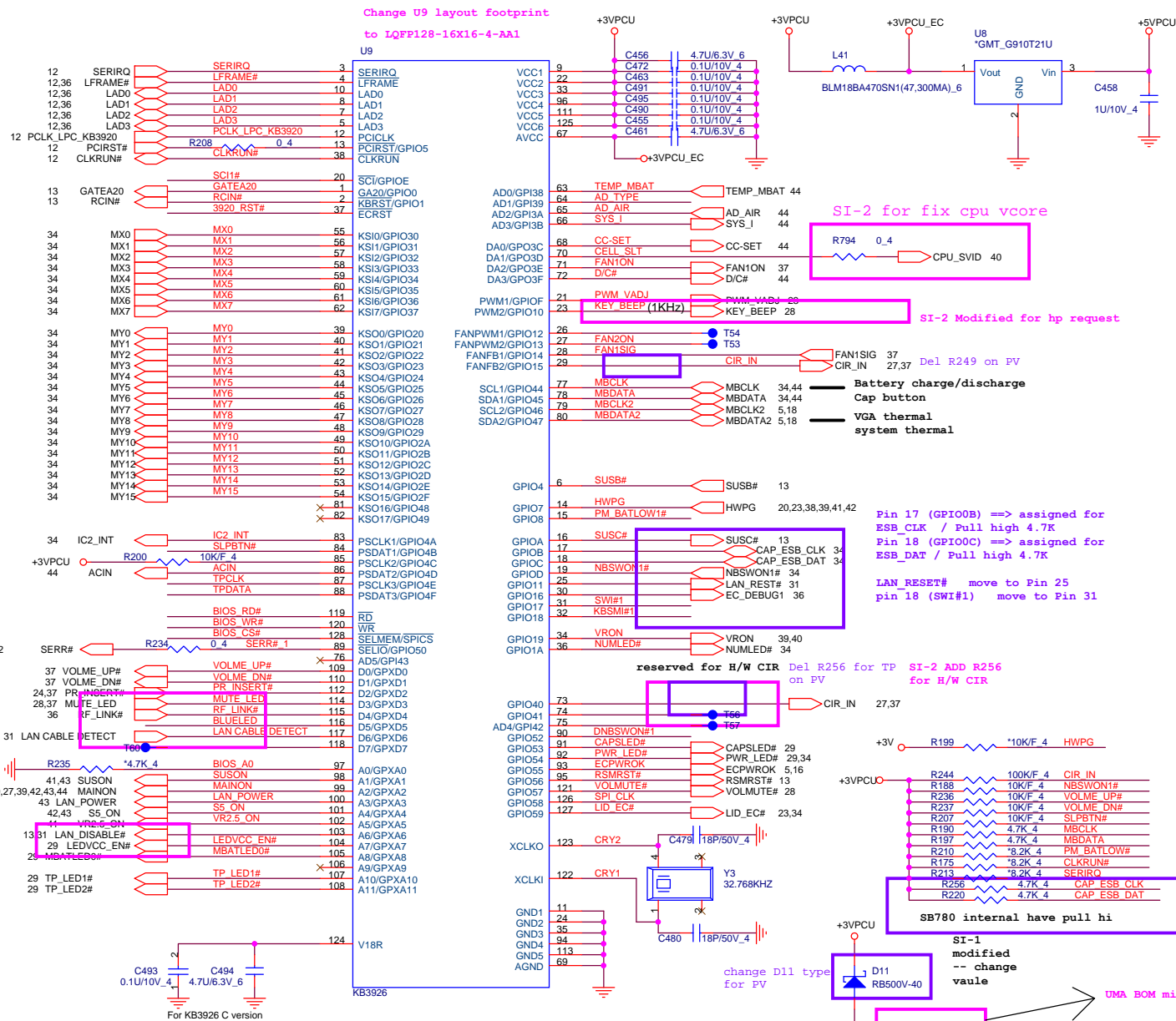
SI-2 Modified



**PROJECT : QT8**  
Quanta Computer Inc.

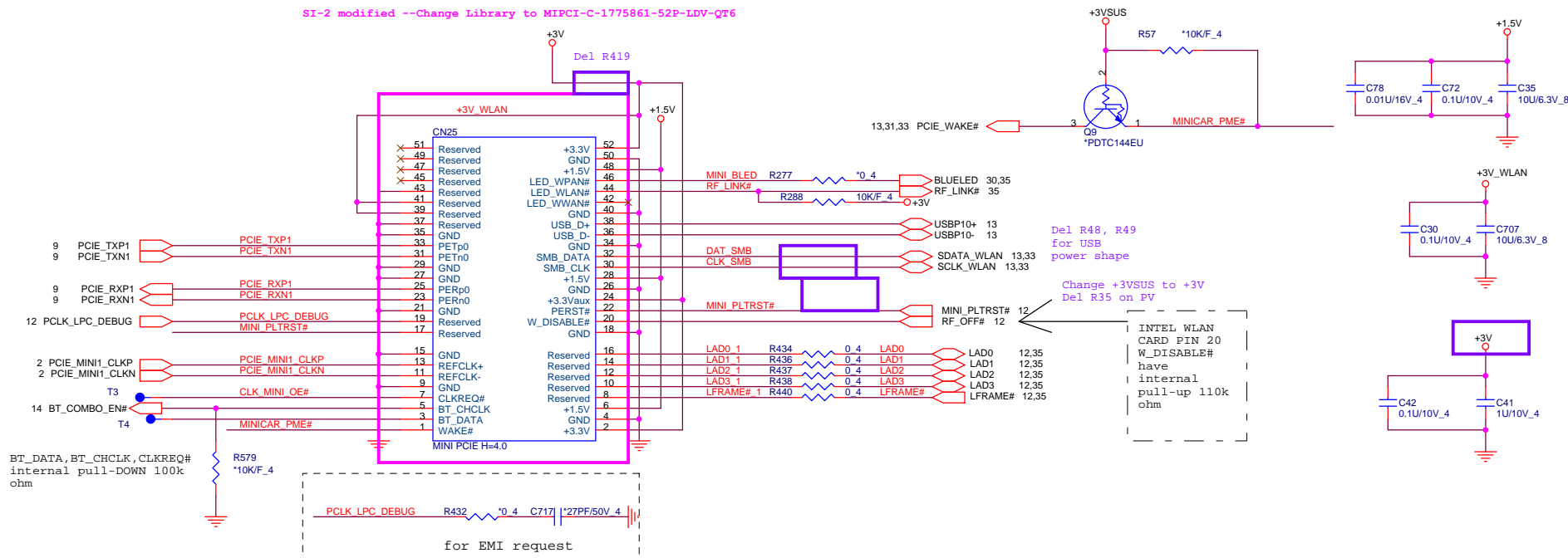
Size Custom Document Number **LED/KEYBOARD/SW** Rev 1A  
Date: Tuesday, February 19, 2008 Sheet 34 of 45

Change U9 layout footprint  
to LQFP128-16X16-4-AA1

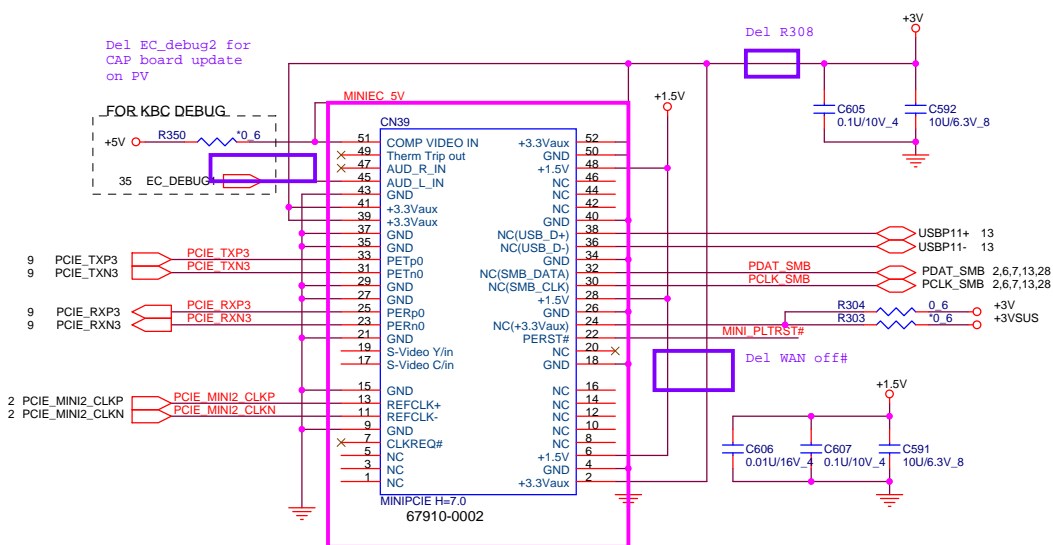


**Mini PCI-E Card 1 WLAN**

SI-2 modified --Change Library to MIPCI-C-1775861-52P-LDV-QT6



**Mini PCI-E Card 2 TV tuner card**



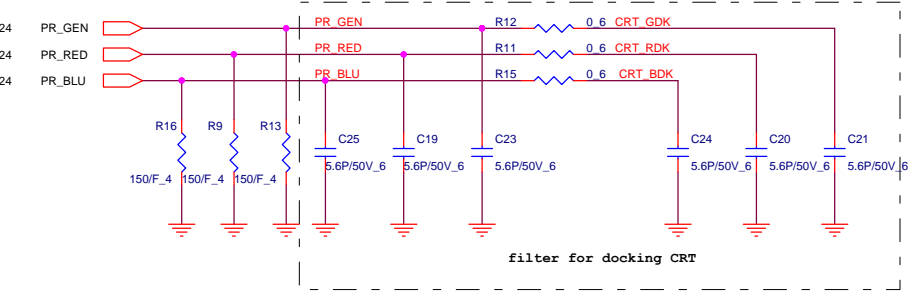
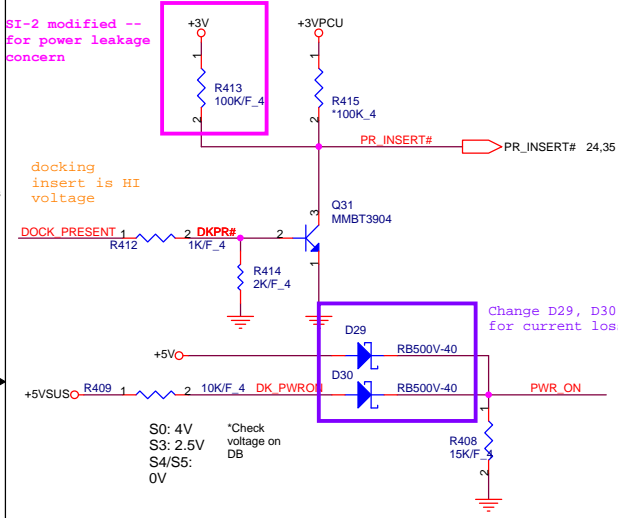
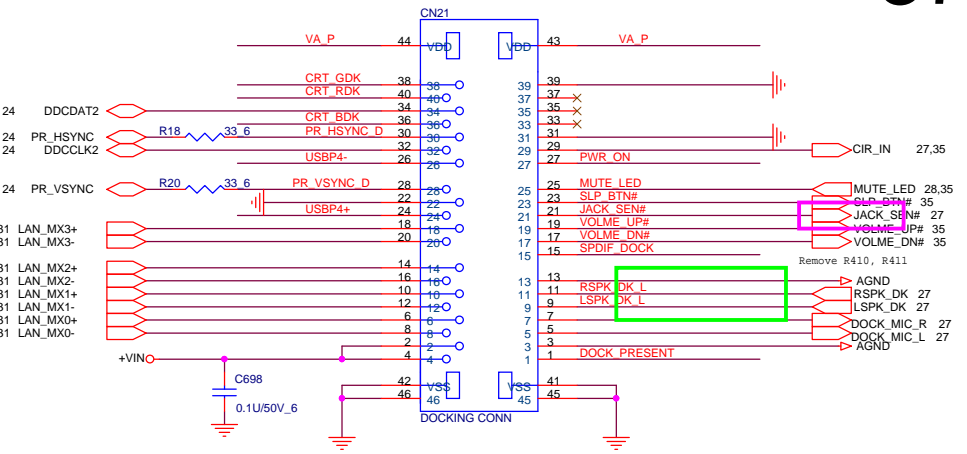
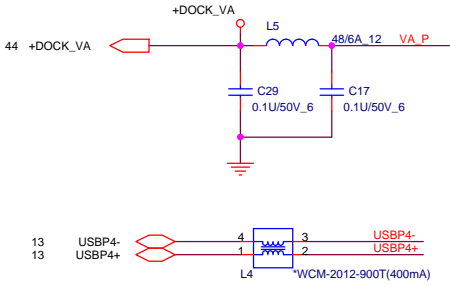
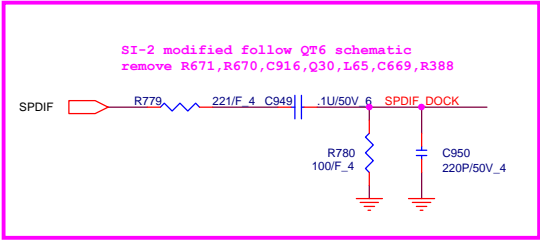
SI-2 modified --Change Library to MIPCIE-P04-FJ504-170-52P-QT6



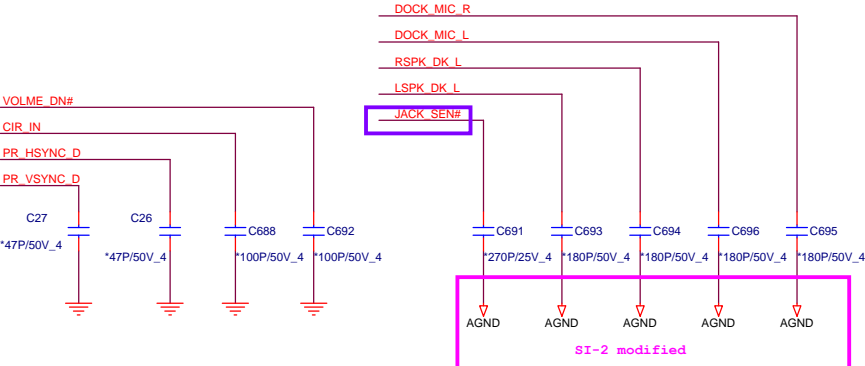
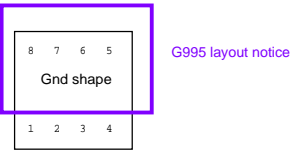
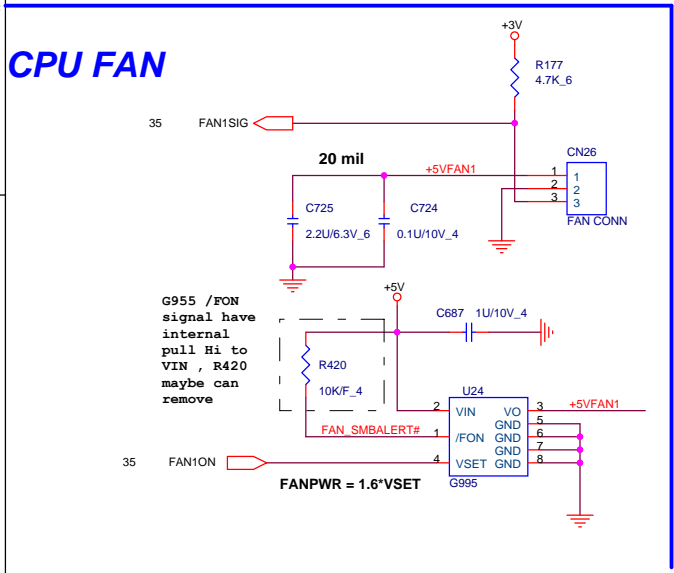
**PROJECT : QT8**  
Quanta Computer Inc.

Size Custom	Document Number <b>Mini CARD X 3</b>	Rev 1/
Date: Tuesday, February 19, 2008		Sheet 36 of 45

support 6A 200mils  
CX000480005



CPU FAN



# DC/DC +3VPCU/+ 5VPCU/ +12VALW

- +5VPCU 27,28,34,35,39,40,41,42,43
- +3VPCU 5,12,23,29,30,34,35,37,40,41,42,44
- +3VSUS 13,25,30,36,39,41,43
- +3VS5 5,7,12,13,14,15,16,23,26,33,43
- +5VSUS 23,30,35,37,43
- +5V 5,15,20,23,24,25,27,28,29,30,33,36,37,39,42,43
- +LANVCC

5 Volt +/- 5%  
**+5VPCU**  
 C/C:8A  
 P/C:10A

TON: 5V / 3.3V  
 GND = 400 / 500KHz  
 REF = 400 / 300KHz  
 VCC = 200 / 300KHz

Place these CAPs  
 close to FETs

Place these CAPs  
 close to FETs

3.3 Volt +/- 5%

**+3VPCU**  
 C/C:8A  
 P/C:10A

$$V_{out} = 0.7(R_a + R_b) / R_b$$

R<sub>b</sub> around 49.9k

SI-1 Modified -  
 ECAP6\_3X6\_1-7\_2-QT8

$$I_{lim} * MOSFET(R_{DS(on)}) = V_{ILIM}(mV) / 10$$

$$V_{ILIM}(mV) = 5uA * R_{ILIM}$$

SI-1 Modified  
 -ECAP6\_3X6\_1-7\_2-QT8

**+3V**  
 6.76A  
**S0-S1**


**+3VSUS**  
 1.84A  
**S0-S3**

**+3VS5**  
 0.5A  
**S0-S5**

**+5VSUS**  
 4.5A  
**S0-S3**

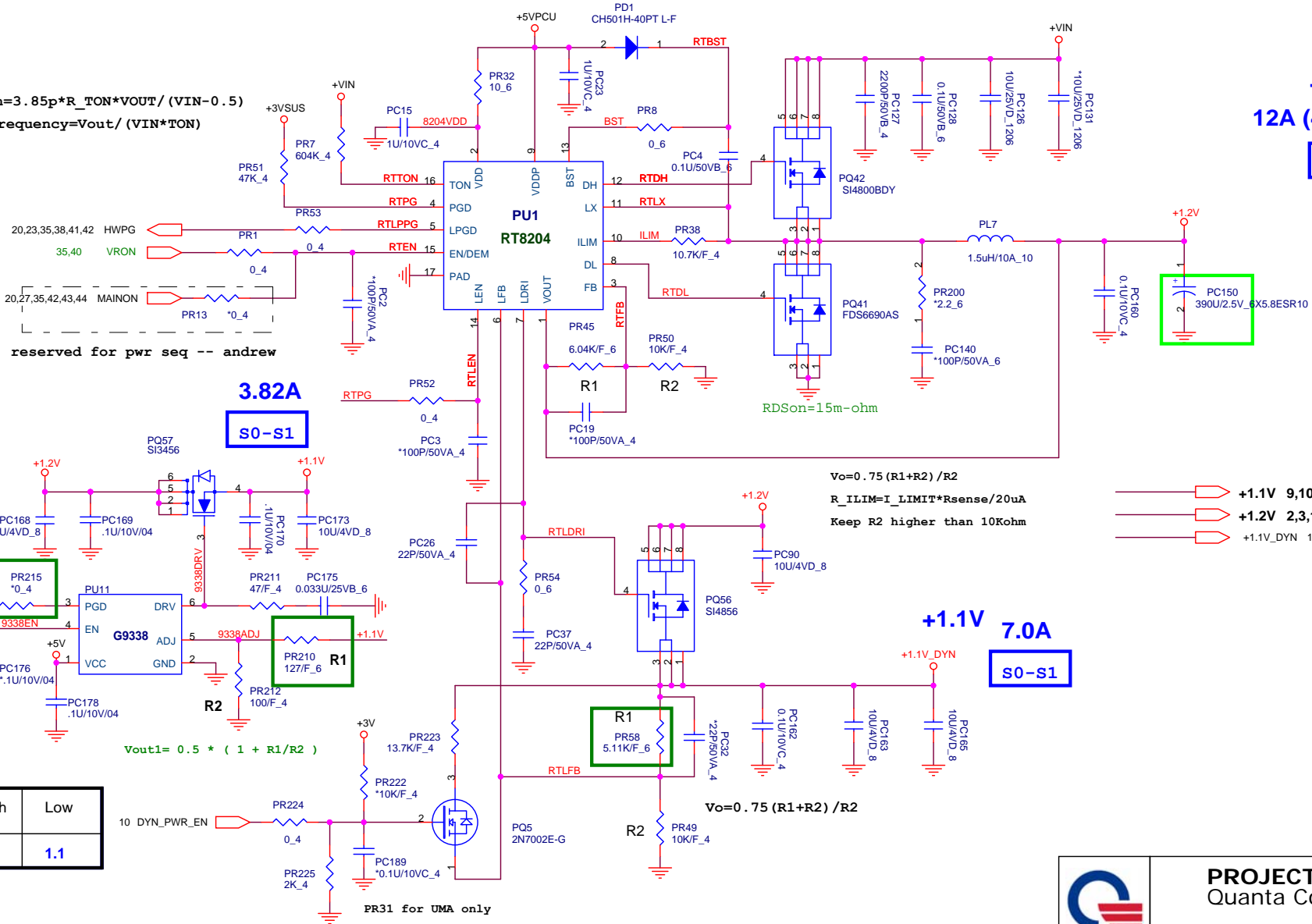
**+5V**  
 4.31A  
**S0-S1**

**+LANVCC**  
 0.27A

	<b>PROJECT : QT8</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number <b>+5V/+3V(ISL6237)</b>	Rev 1A
Date: Tuesday, February 19, 2008		Sheet 38 of 45	

$$T_{on} = 3.85p \cdot R_{TON} \cdot V_{OUT} / (V_{IN} - 0.5)$$

$$Frequency = V_{out} / (V_{IN} \cdot T_{ON})$$



**PROJECT : QT8**  
**Quanta Computer Inc.**

Size B	Document Number <b>+1.2V &amp; +1.1V(RT8204)</b>	Rev 1A
Date: Tuesday, February 19, 2008	Sheet 39 of 45	



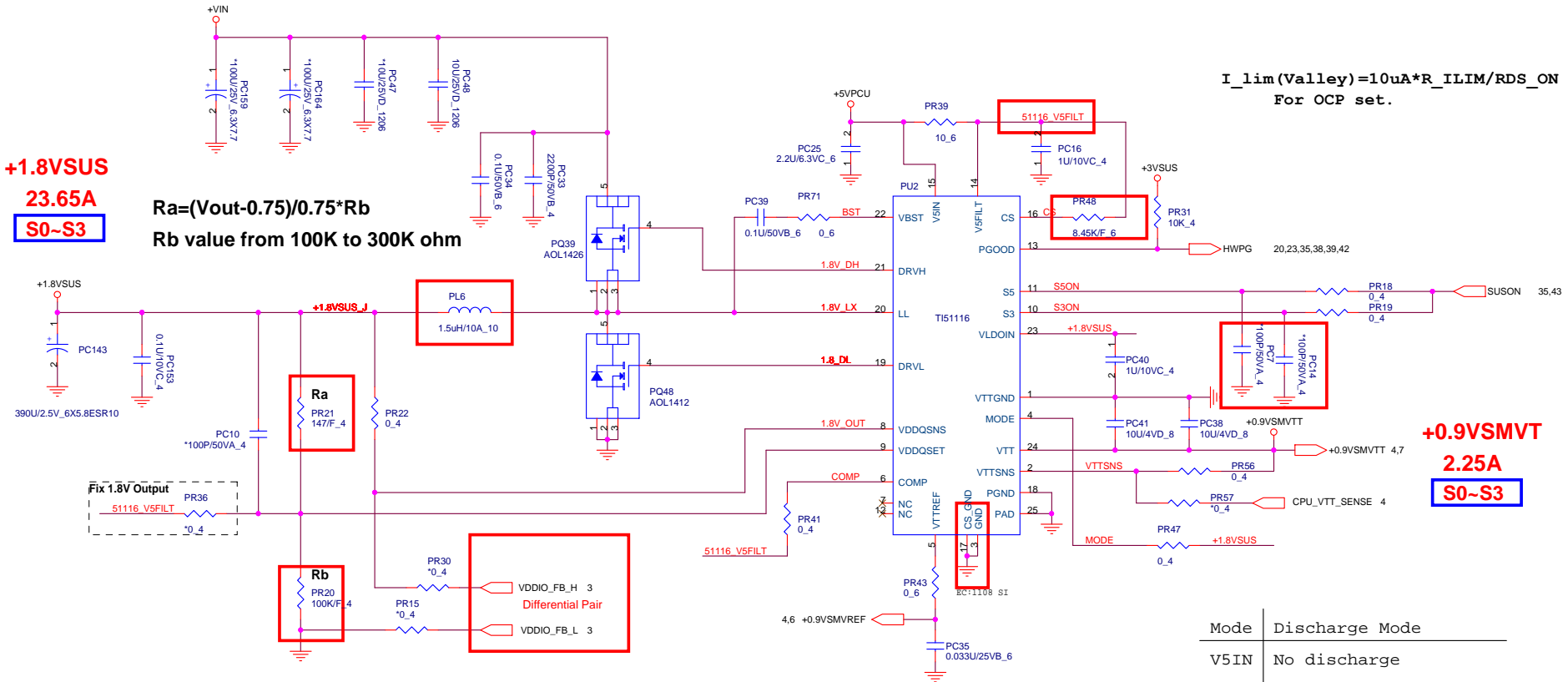


+2.5V 3  
+1.8VSUS 3,4,5,6,7,40,42,43

$I_{lim(Valley)} = 10\mu A * R_{ILIM}/R_{DS\_ON}$   
For OCP set.

+1.8VSUS  
23.65A  
S0~S3

$R_a = (V_{out} - 0.75) / 0.75 * R_b$   
 $R_b$  value from 100K to 300K ohm



+0.9VSMVT  
2.25A  
S0~S3

+2.5V  
0.25A  
S0~S1

For EMI-SI

+1.8V  
10.4A  
S0~S1

For EMI-SI

Discrete: SI4856  
UMA: SI4800

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

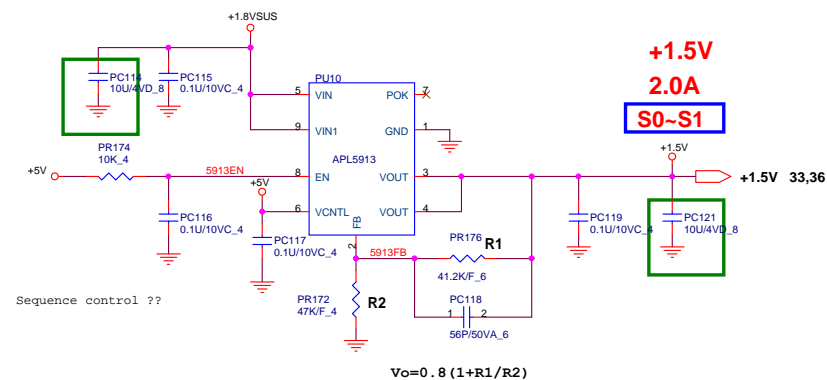
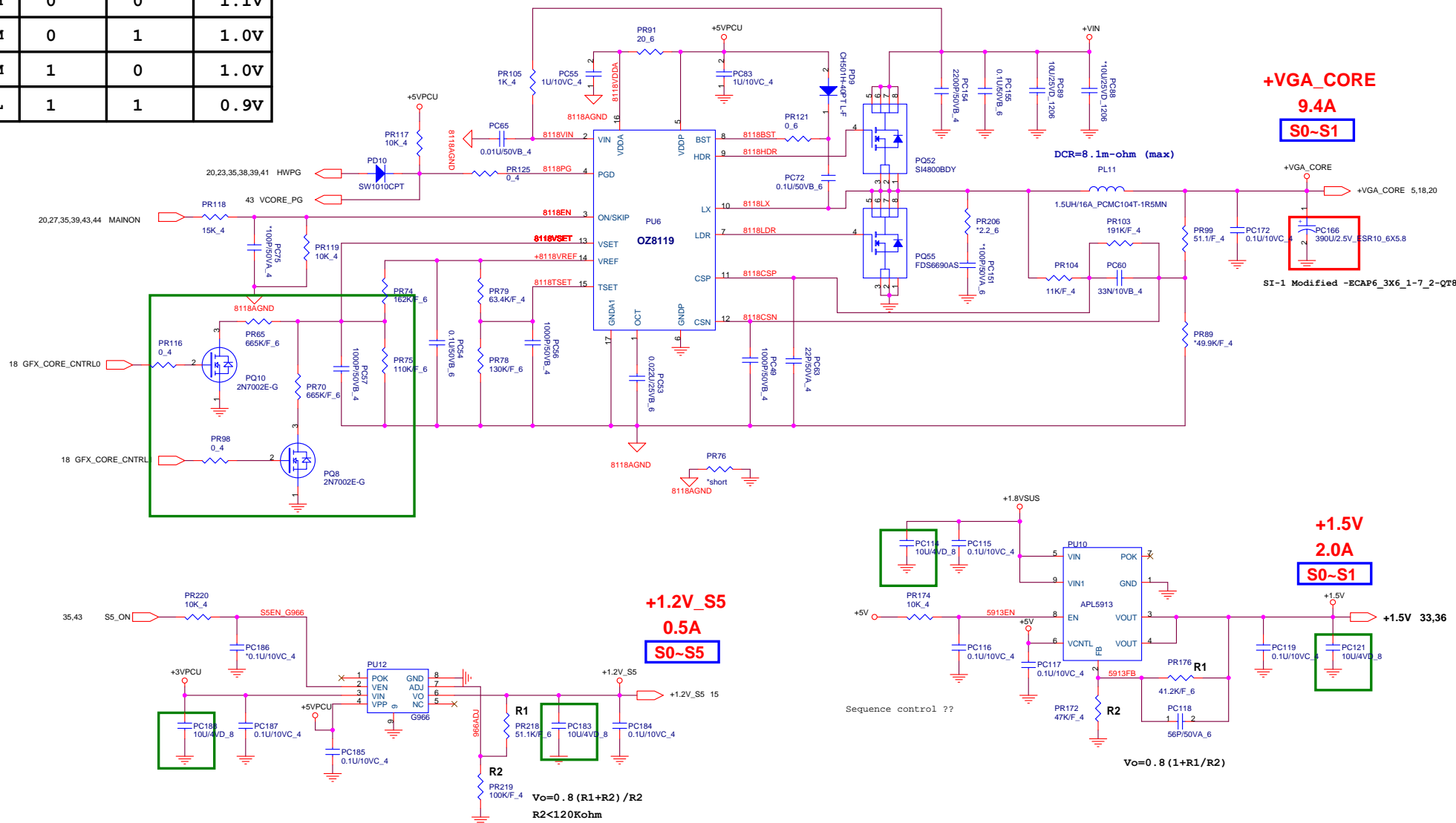
$$V_{TRIP}(mV) = R_{TRIP}(Kohm) * 10(\mu A)$$

$$I_{OCP} = V_{trip}/R_{ds\_on} + I_{Ripple}/2$$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_{\_vddqsns}/2$	DDR
V5IN	1.8	$V_{\_vddqsns}/2$	DDR2
FB	adjustable	$V_{\_VDDQSNS}/2$	$1.5V < VDDQ < 3V$

ATI M82-SE

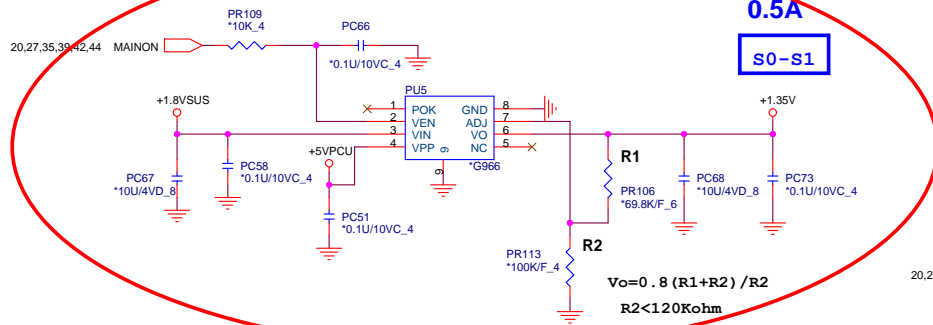
PWRCNTL1	PWRCNTL0	V-CORE
0	0	1.1V
0	1	1.0V
1	0	1.0V
1	1	0.9V



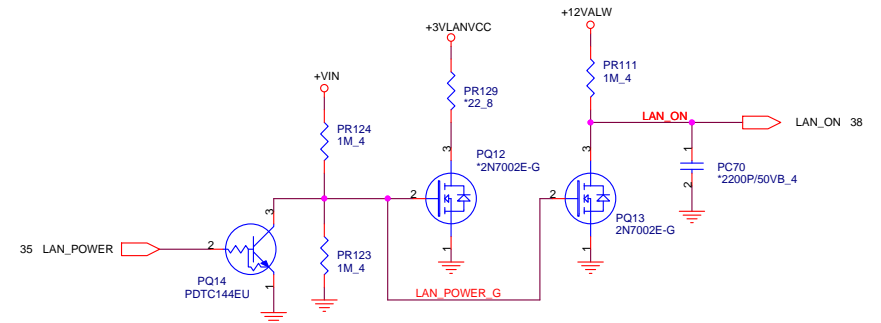
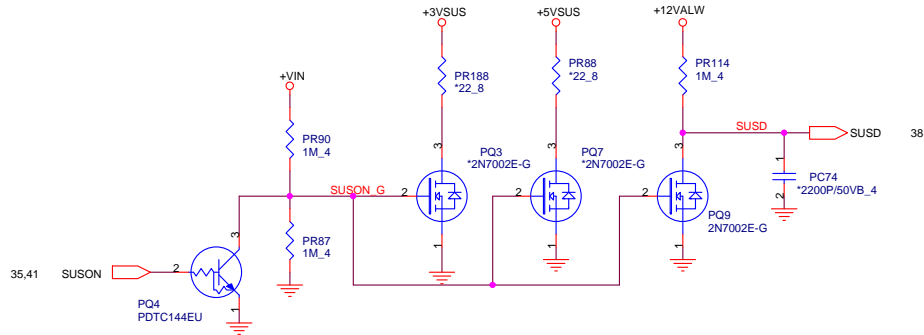
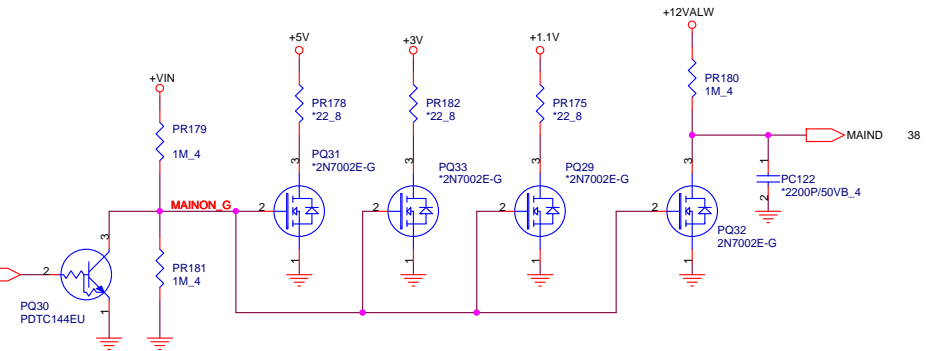
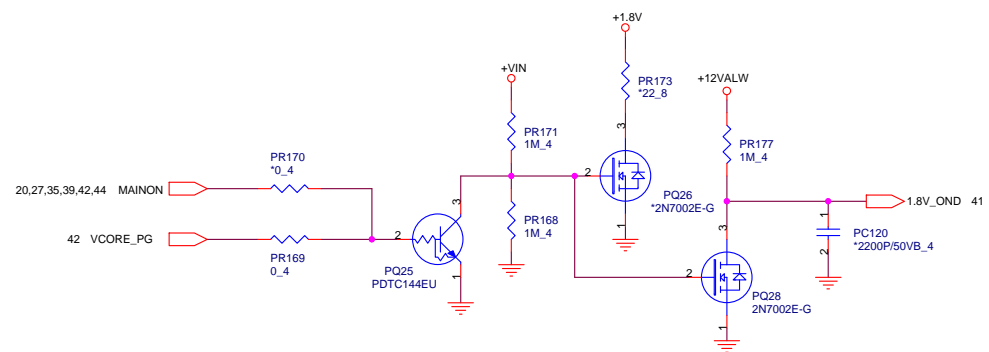
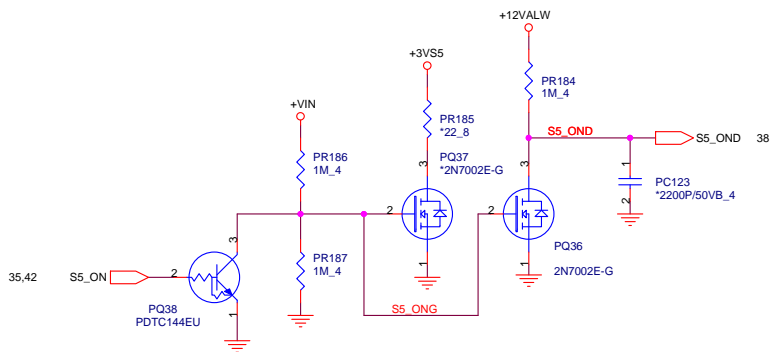
SI-1 Modified - can remove +1.35V for AMD update

0.5A

S0-S1



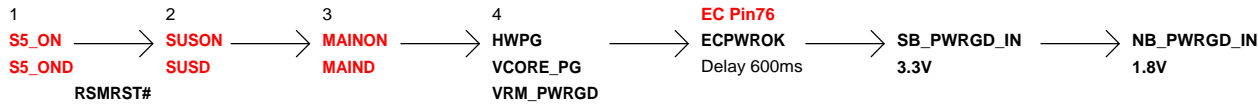
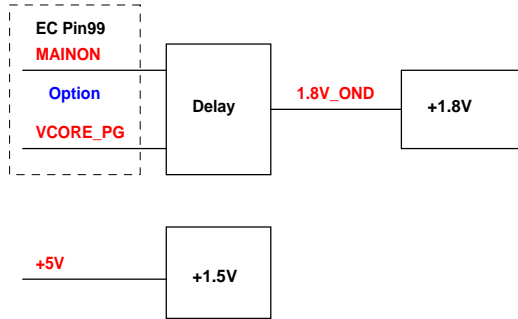
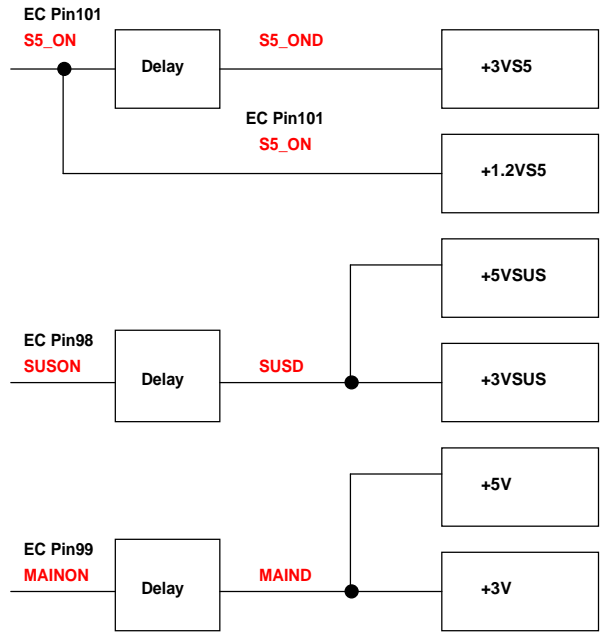
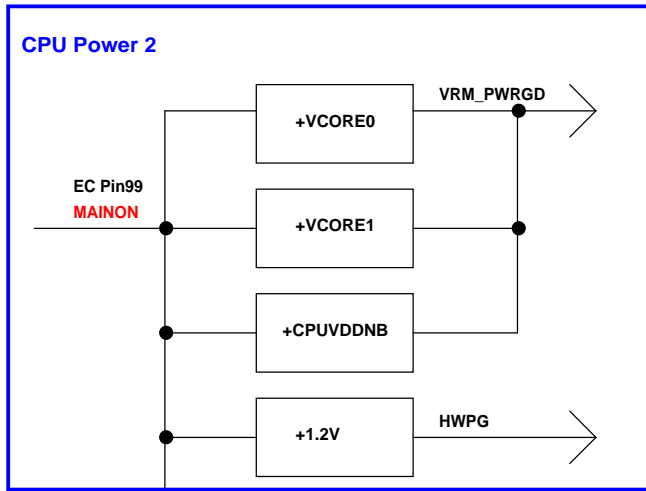
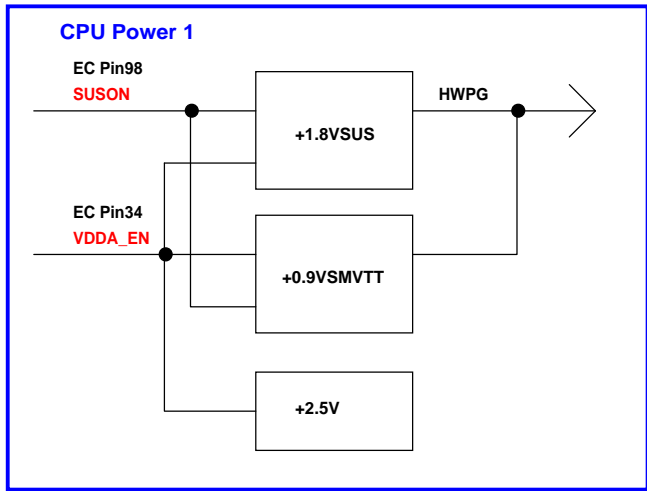
20,27,35,39,42,44 MAINON

*For Discrete Only*

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